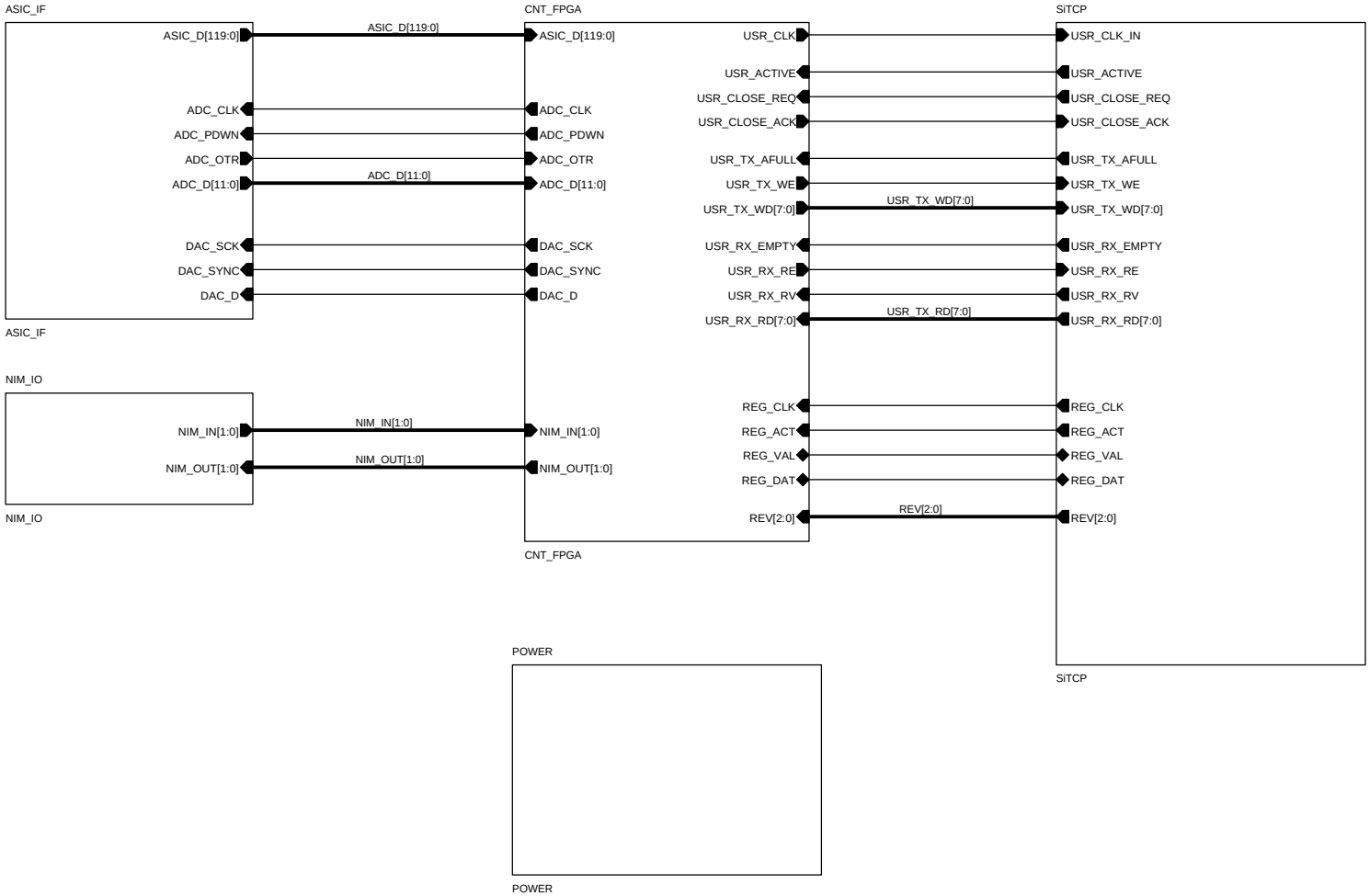
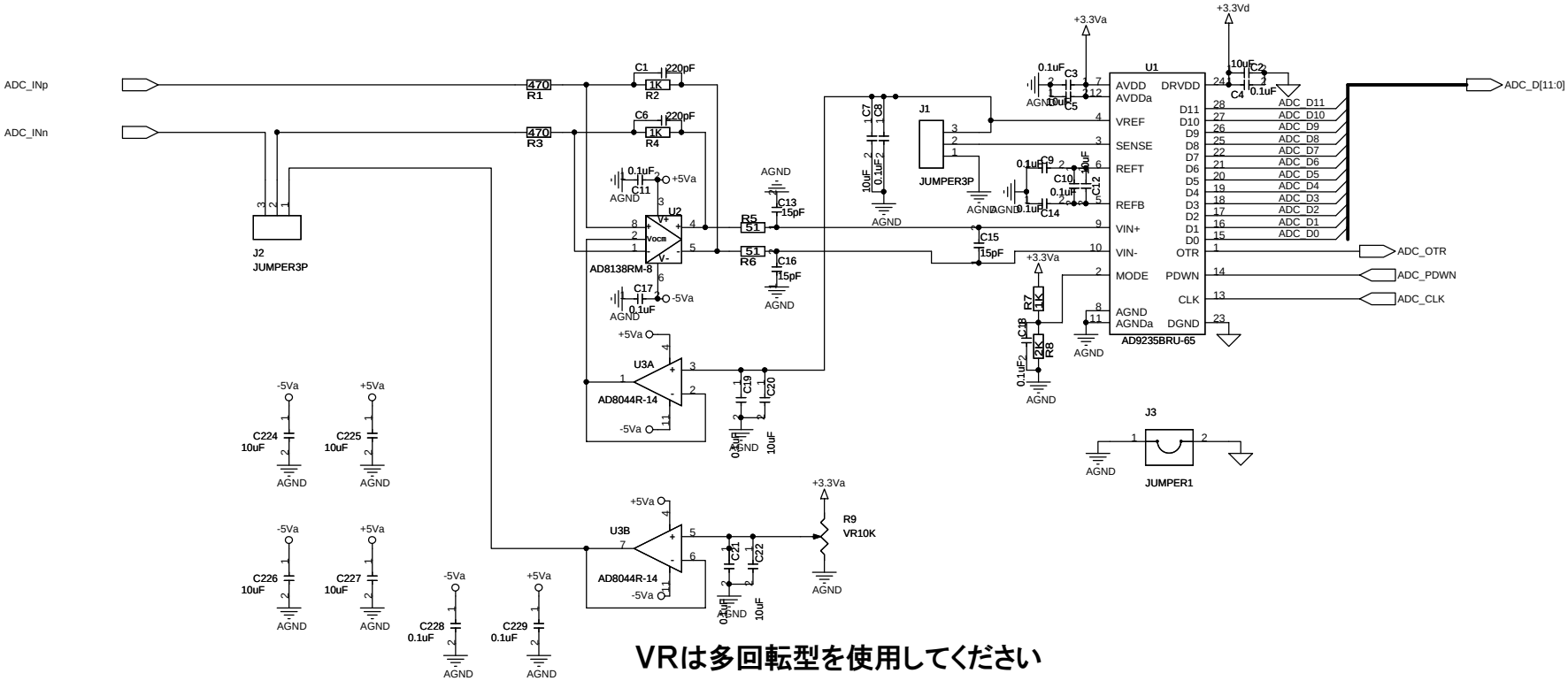


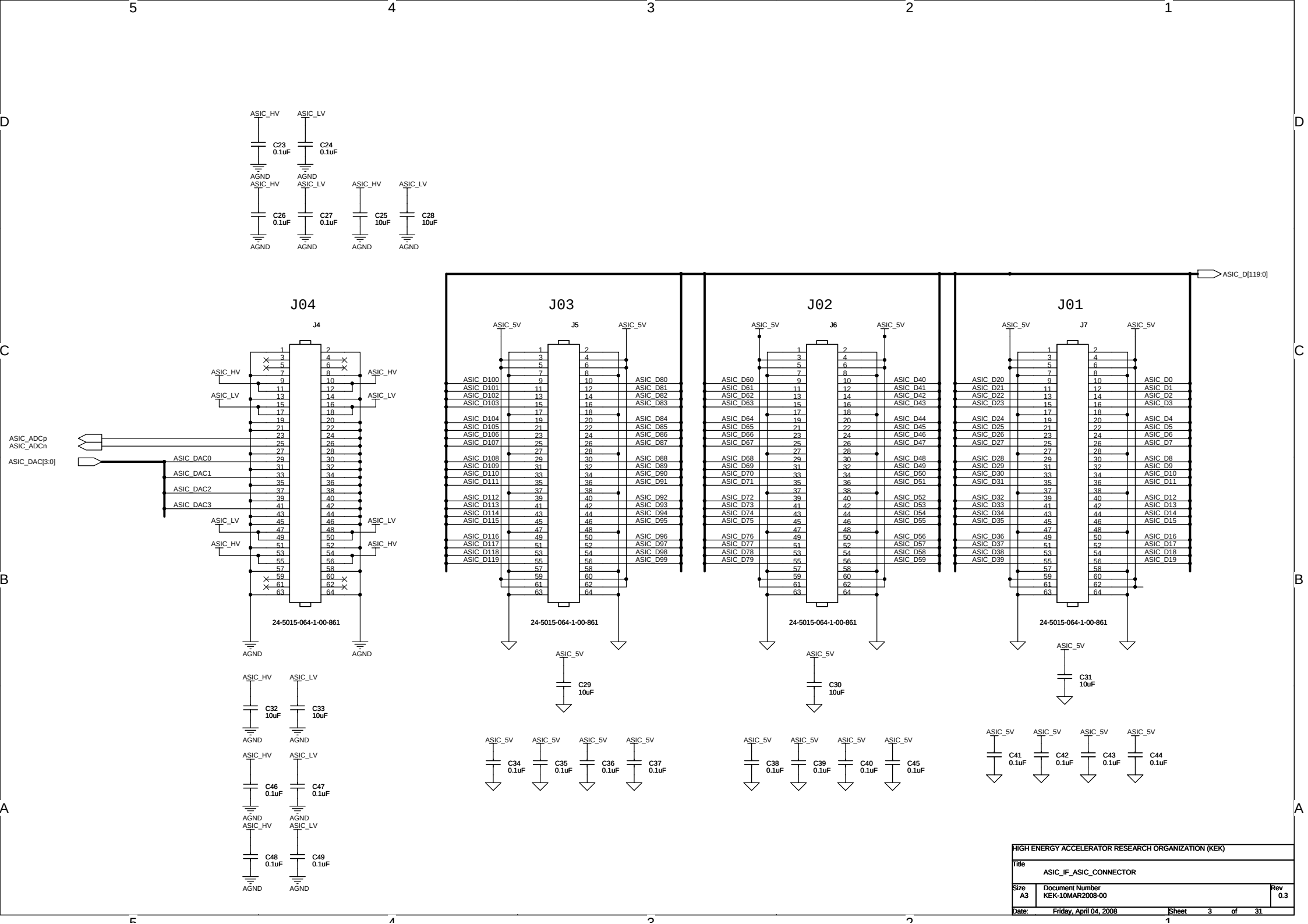
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: TOP (SOIPIX_SITCP)		
Size: A3	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 1 of 31	



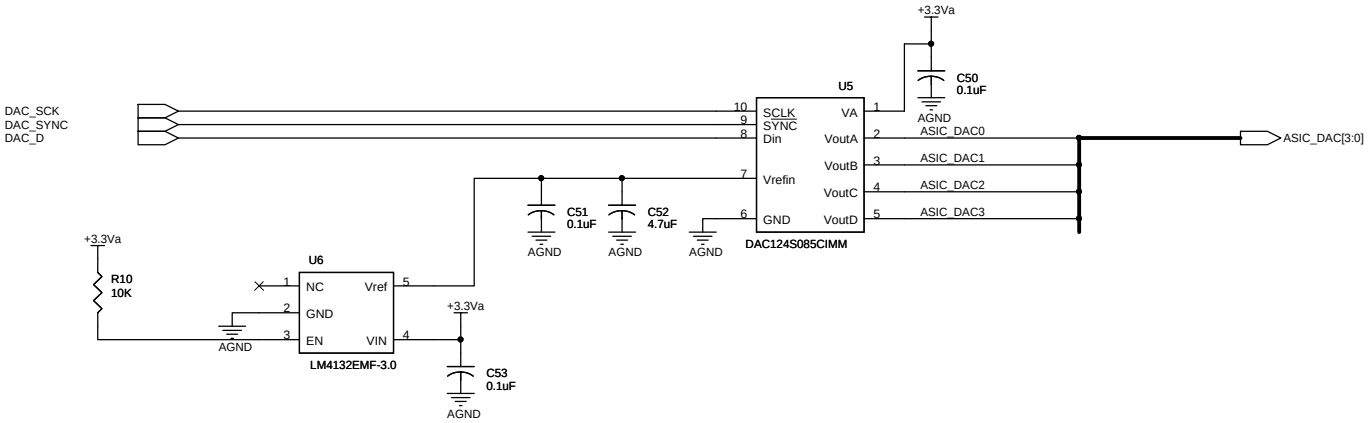
VRは多回転型を使用してください

このページのAD8044は同一パッケージ内のものを使用してください

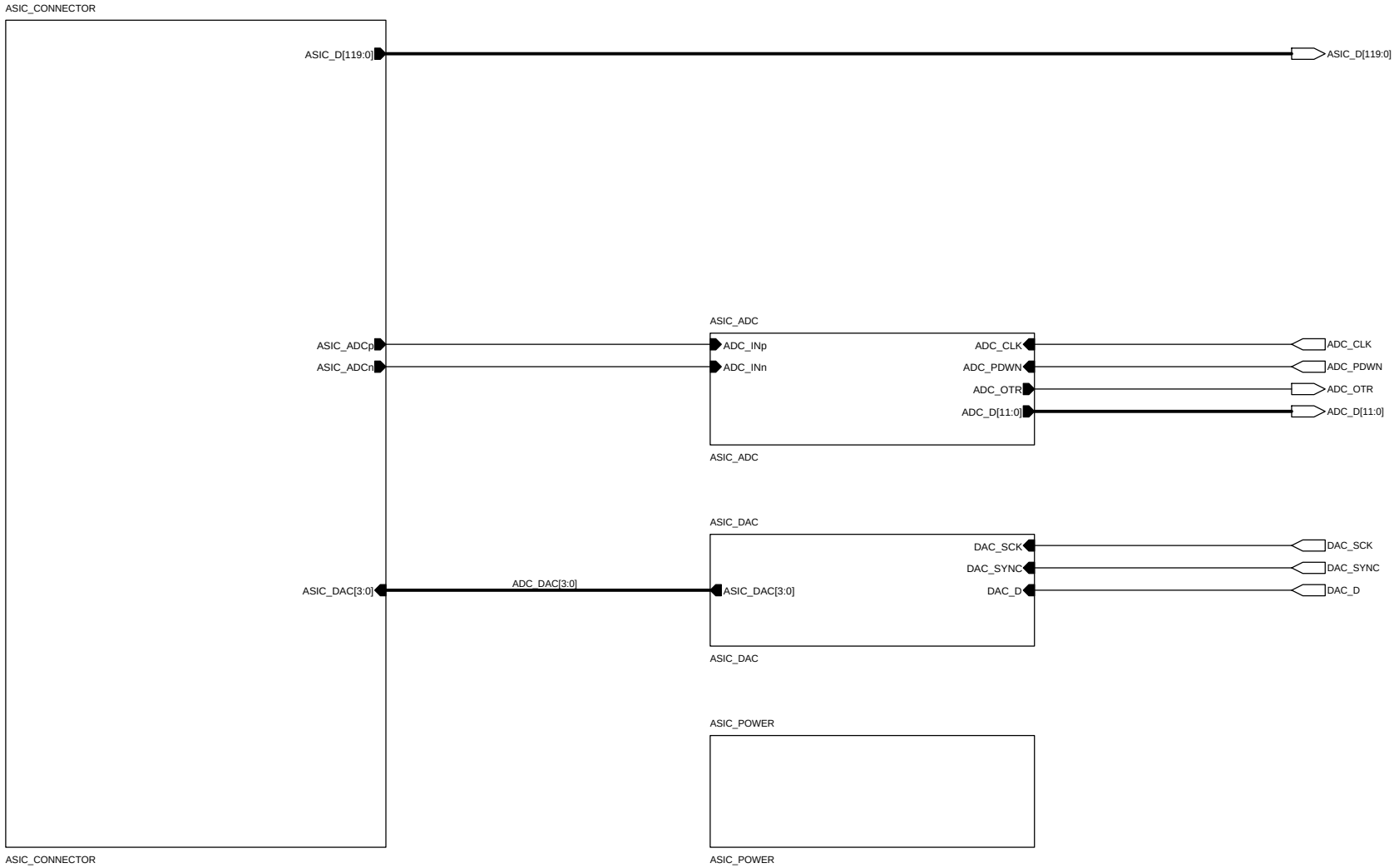
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: ASIC_IF/ASIC_ADC		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Sunday, April 06, 2008	Sheet 2 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)	
Title: ASIC_IF_ASIC_CONNECTOR	
Size: A3	Document Number: KEK-10MAR2008-00 — Rev: 0.3
Date: Friday, April 04, 2008	Sheet 3 of 31



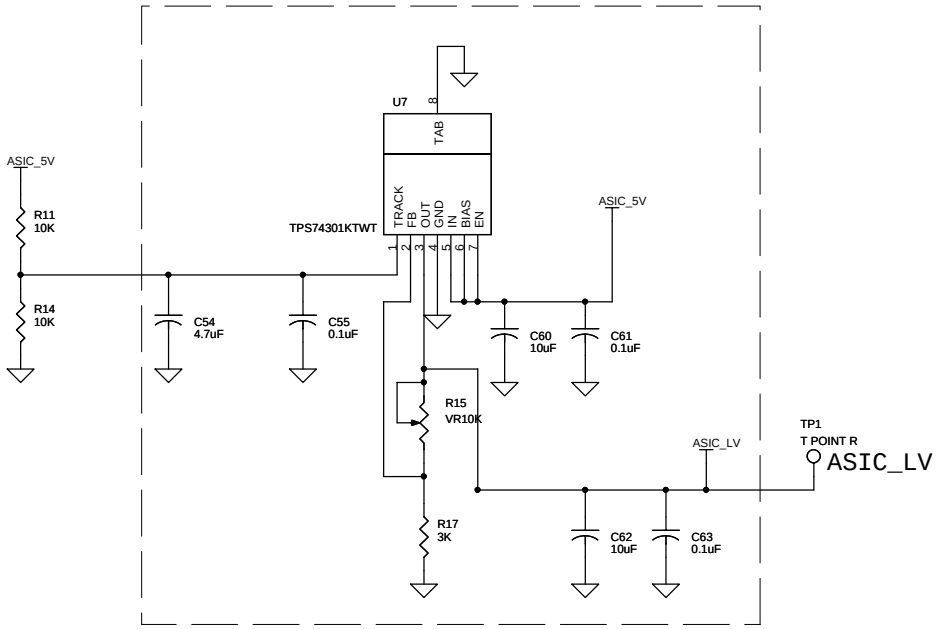
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: ASIC_IF/ASIC_DAC		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 4 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: ASIC_IF		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 5 of 31	

For Low Voltage

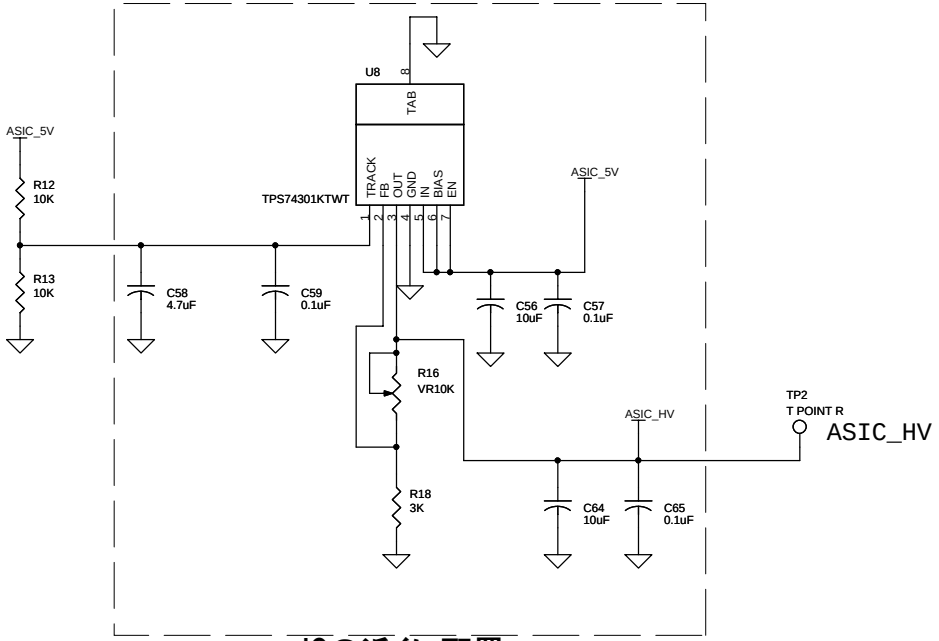
TABは放熱板です
必ず複数ビアで内層GNDへ落としてください。



ICの近くに配置
VRは多回転型を使用してください

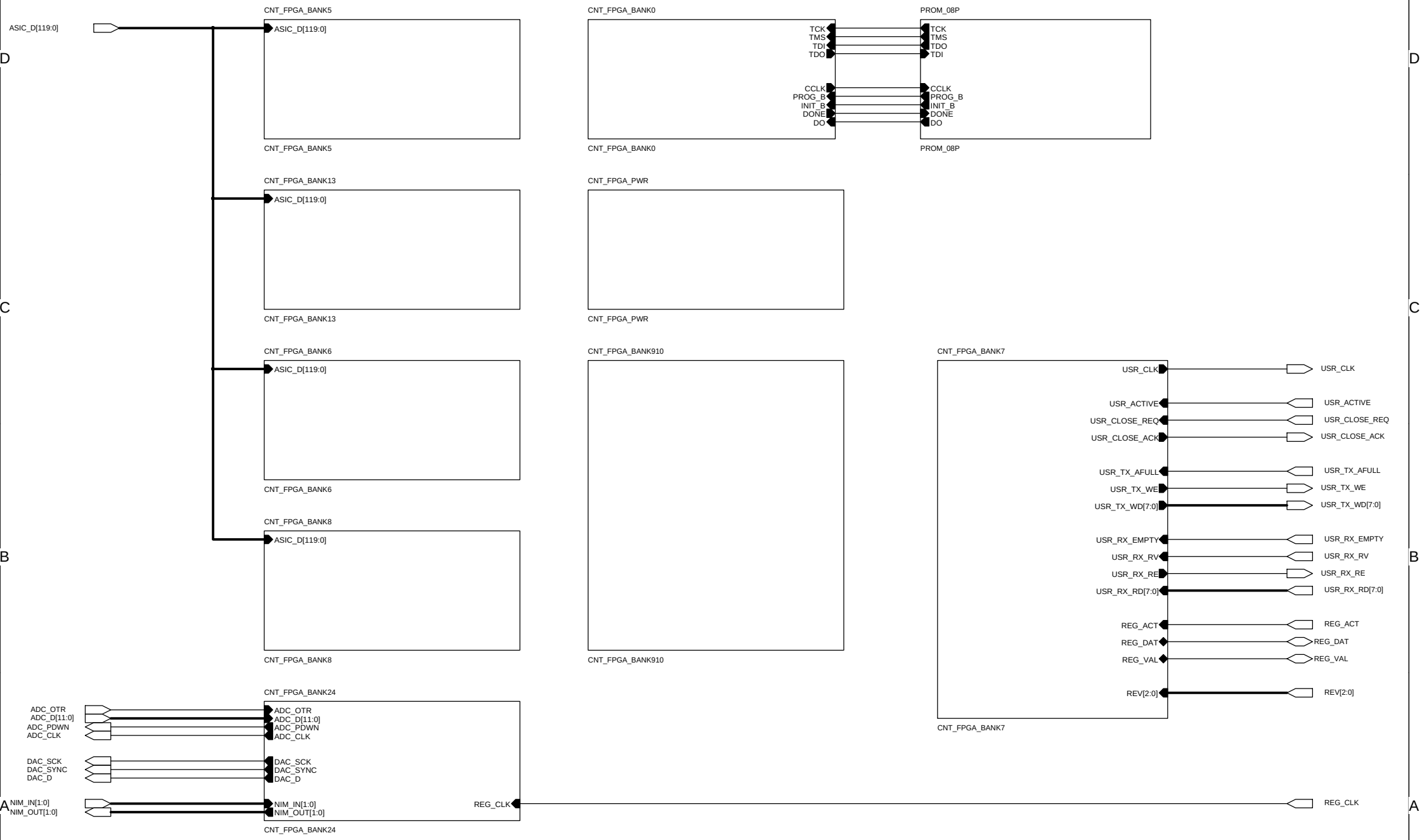
For High Voltage

TABは放熱板です
必ず複数ビアで内層GNDへ落としてください。

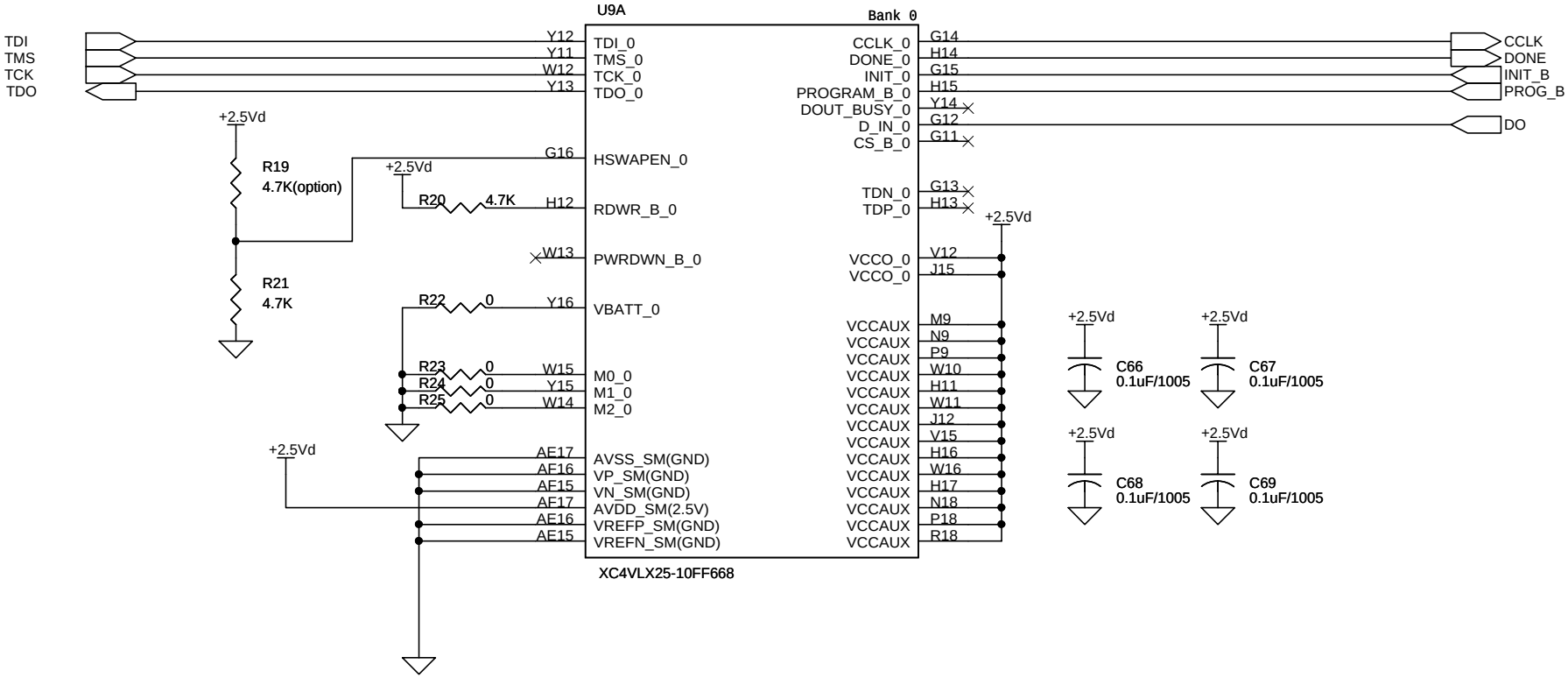


ICの近くに配置
VRは多回転型を使用してください

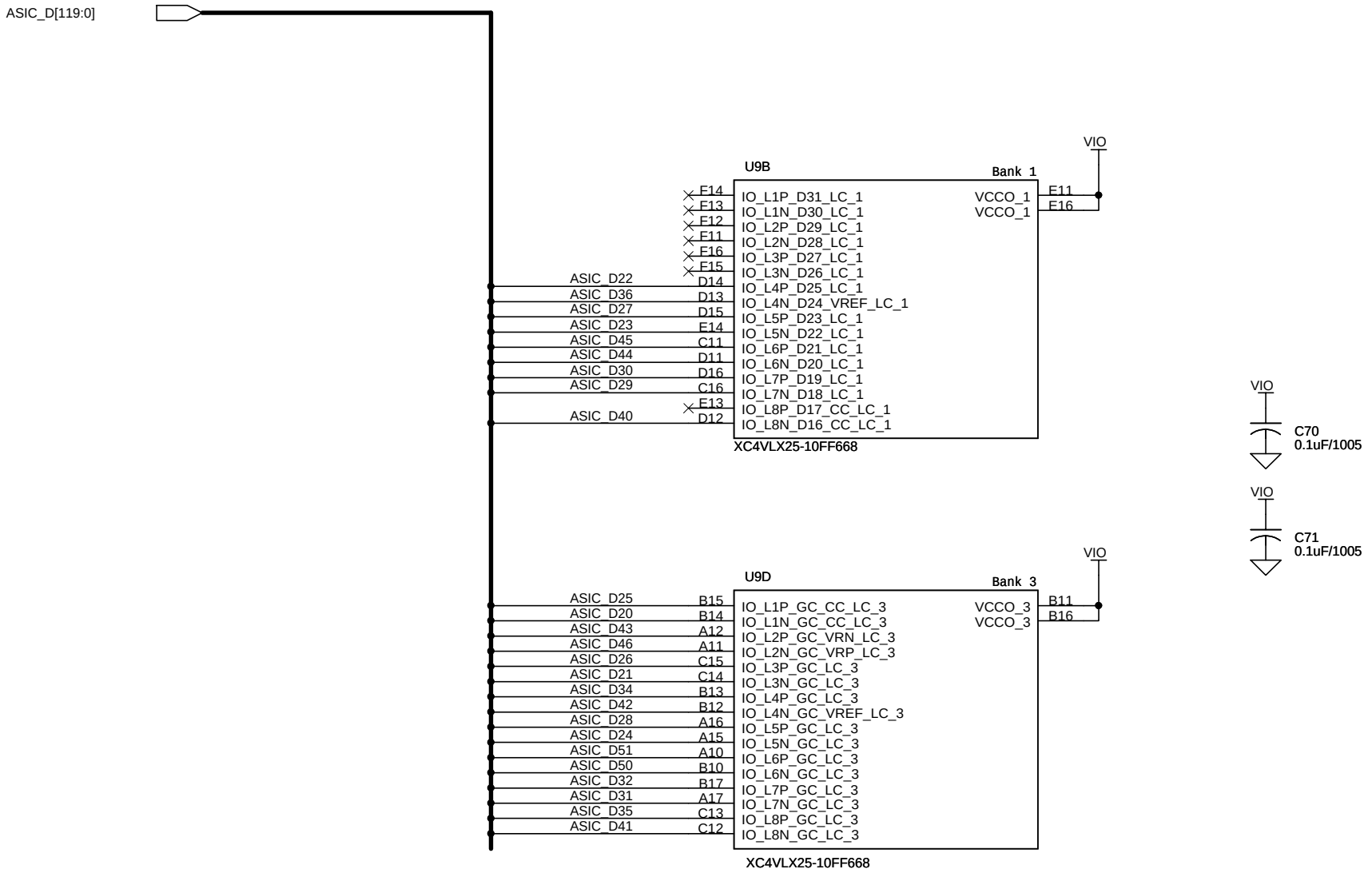
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: ASIC_IF/ASIC_POWER		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 6 of 31	



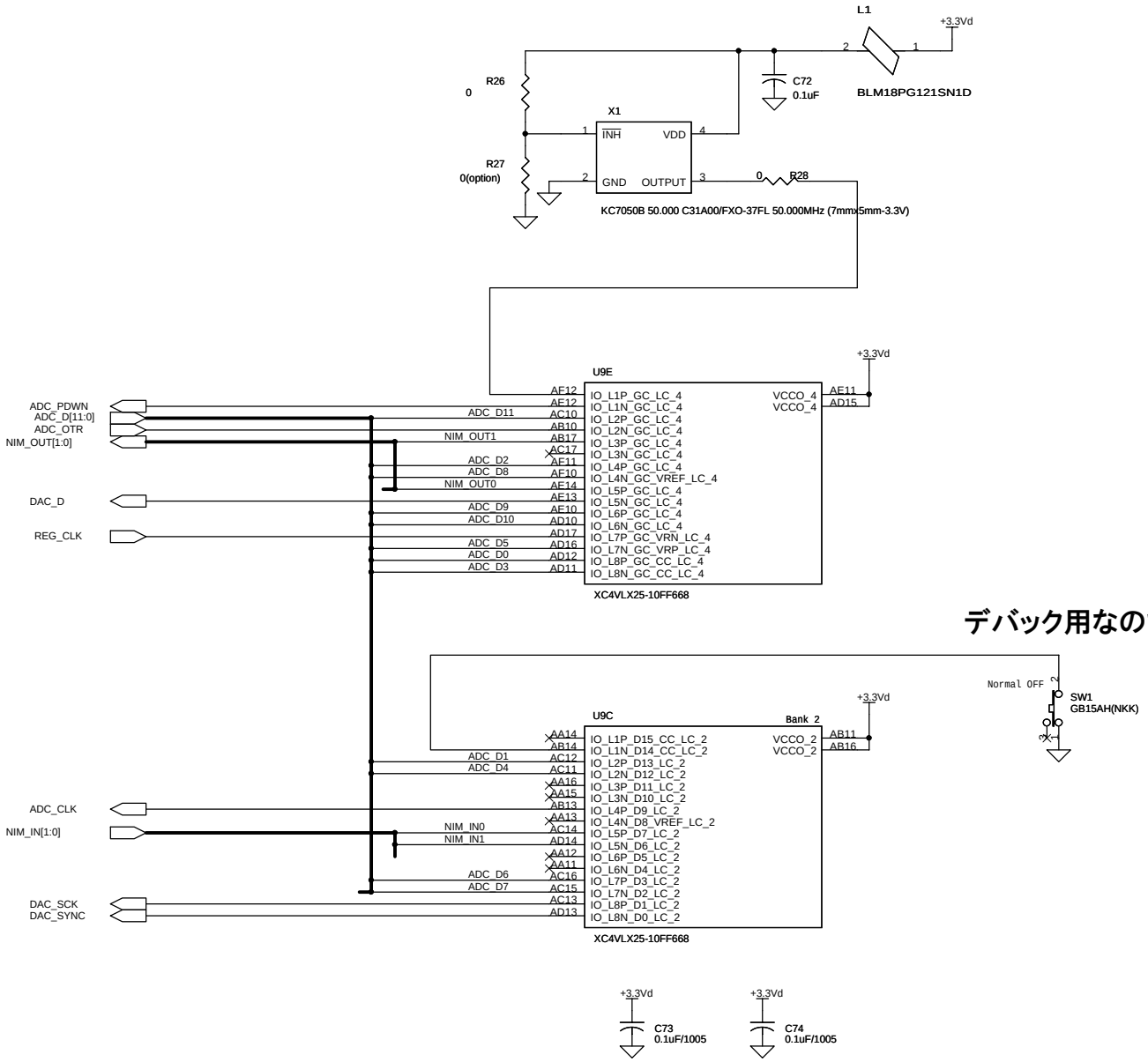
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 7 of 31	



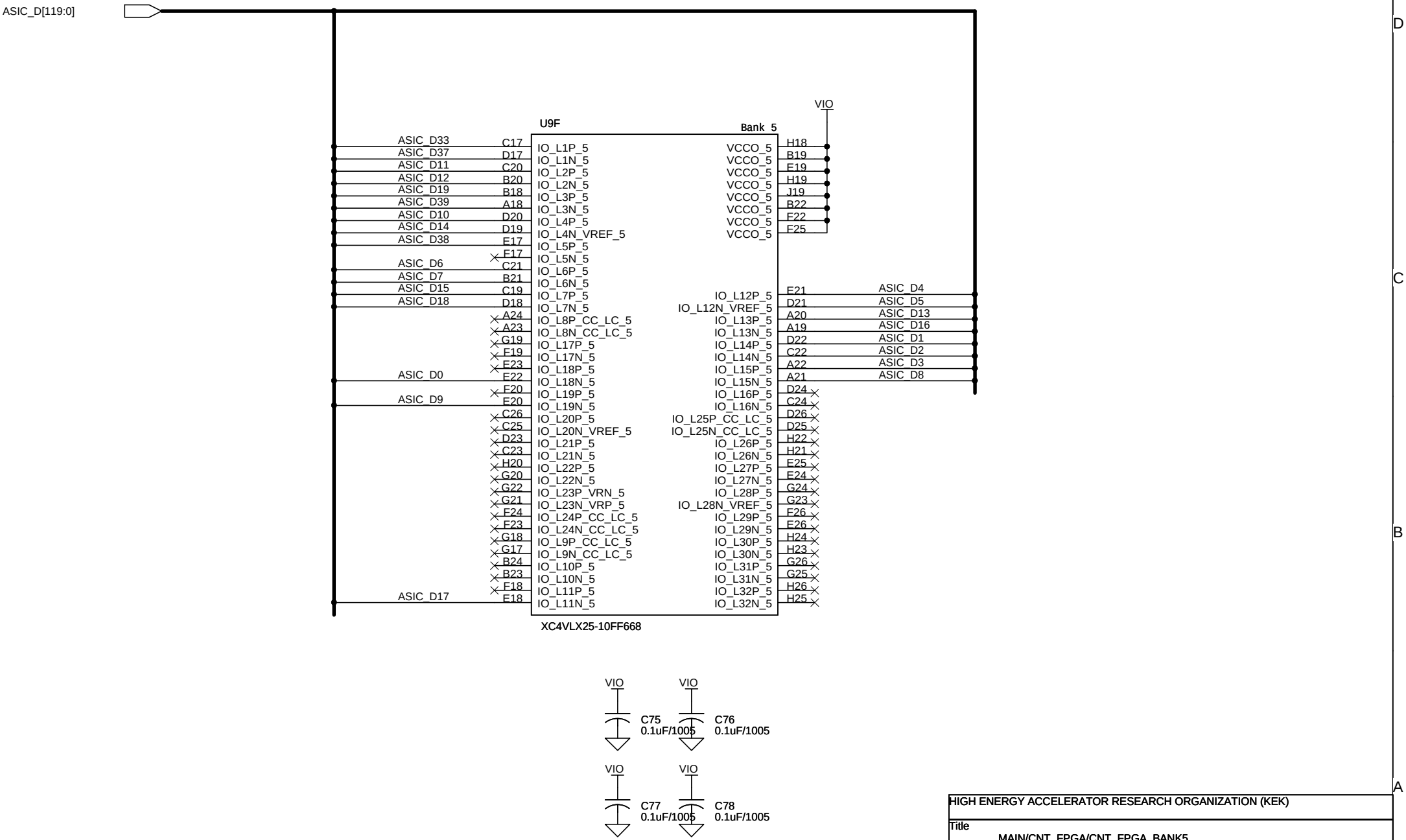
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK0		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 8 of 31	



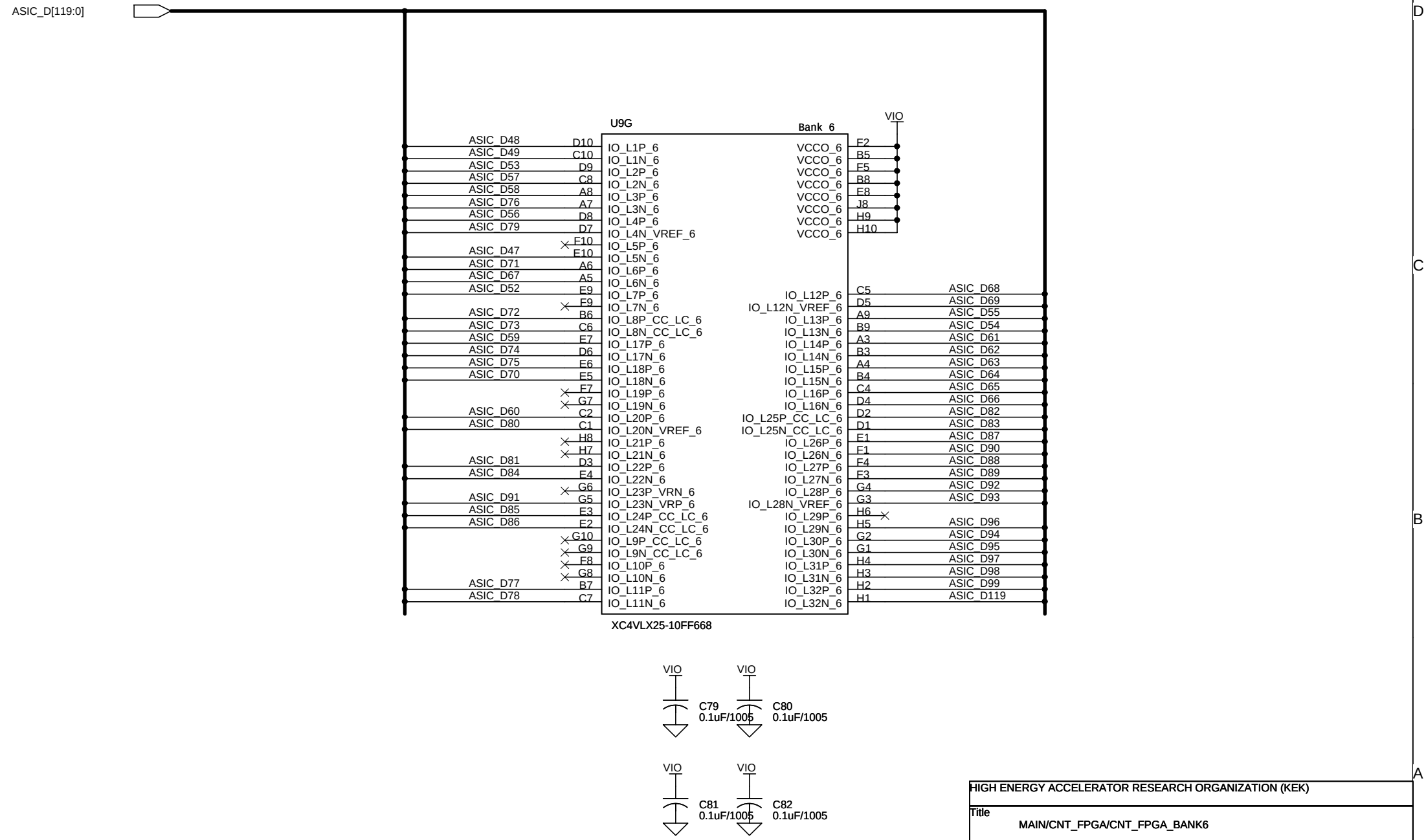
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK13		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 9 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK24		
Size: A3	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 10 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK5		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 11 of 31	



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Title: MAIN/CNT_FPGA/CNT_FPGA_BANK6		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 12 of 31	

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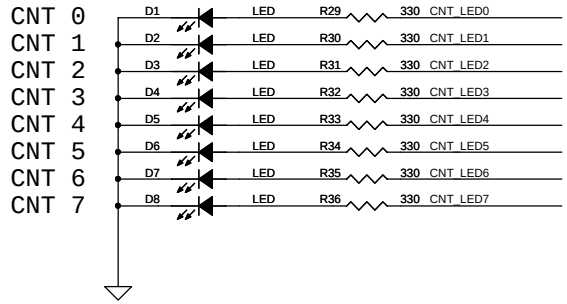

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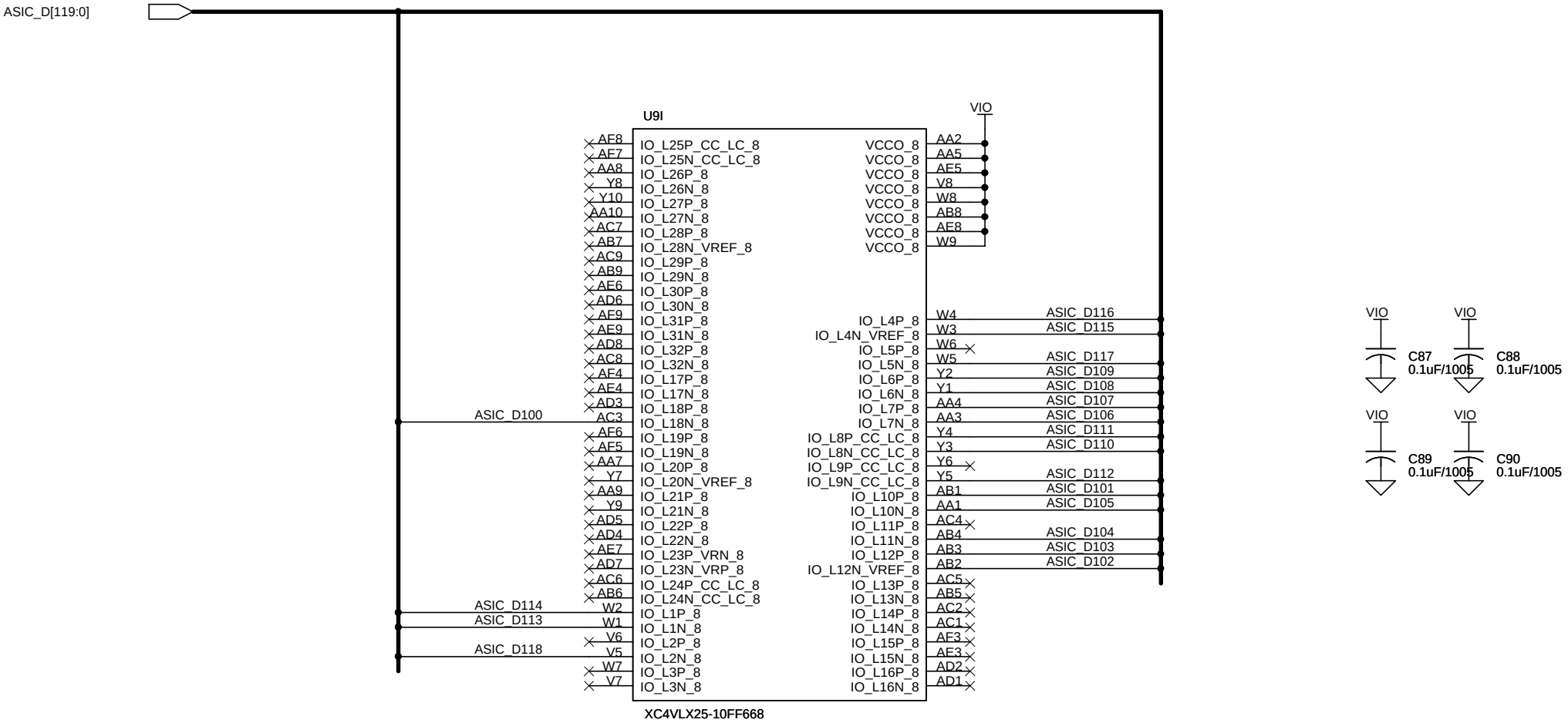
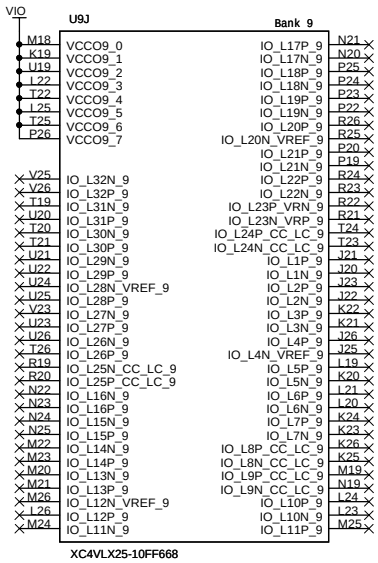
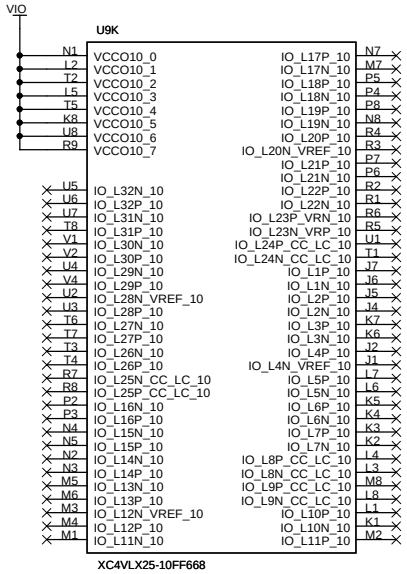
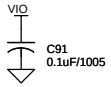
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK7		
Size: A3	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 13 of 31	

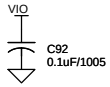


HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK8		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 14 of 31	





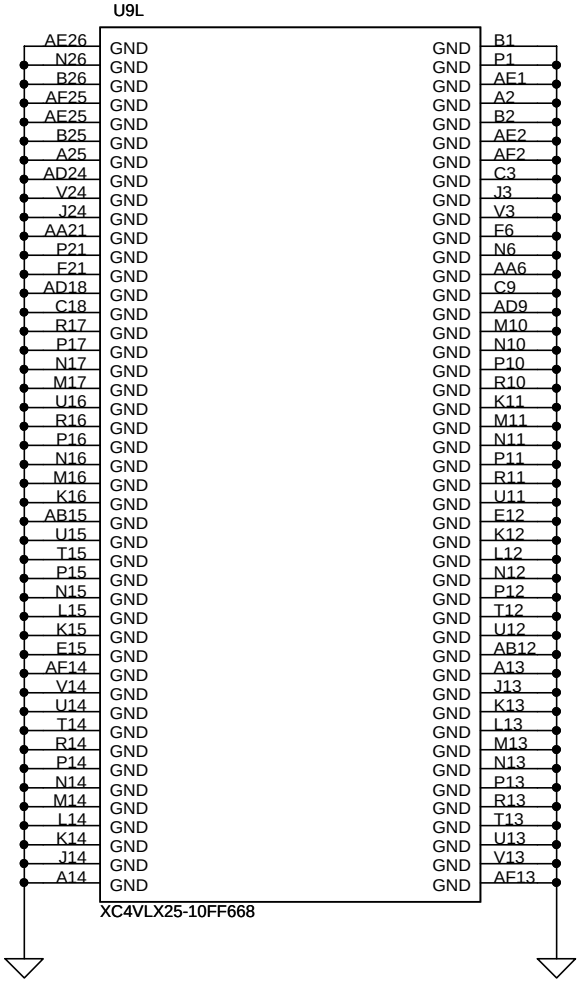


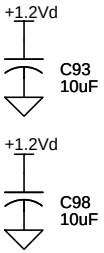


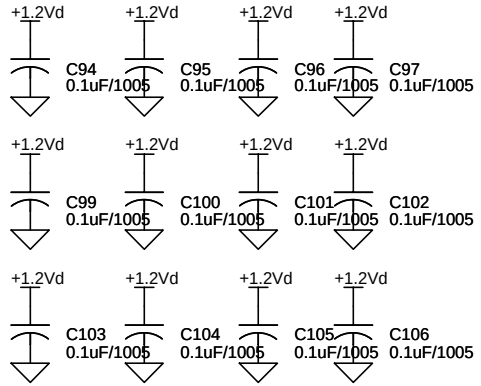
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_BANK9		
Size: A3	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 15 of 31	

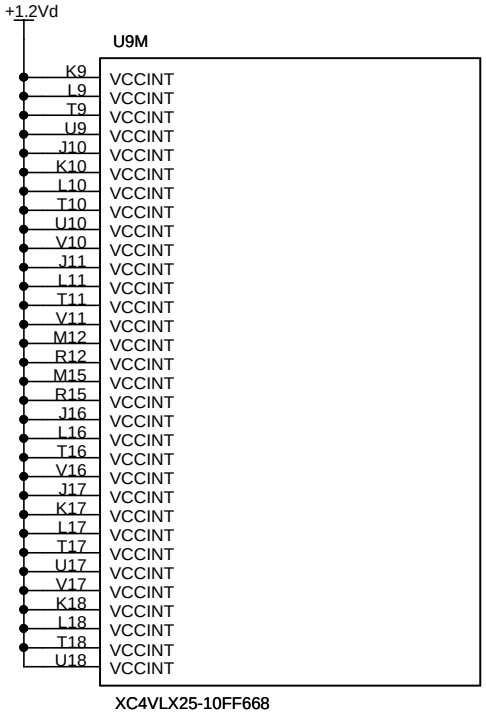
パスコンは多めに置いてあります。

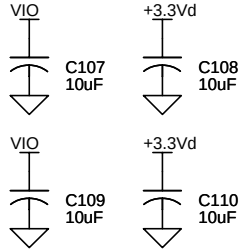
無理しておく必要はありませんので、厳しい時は連絡ください



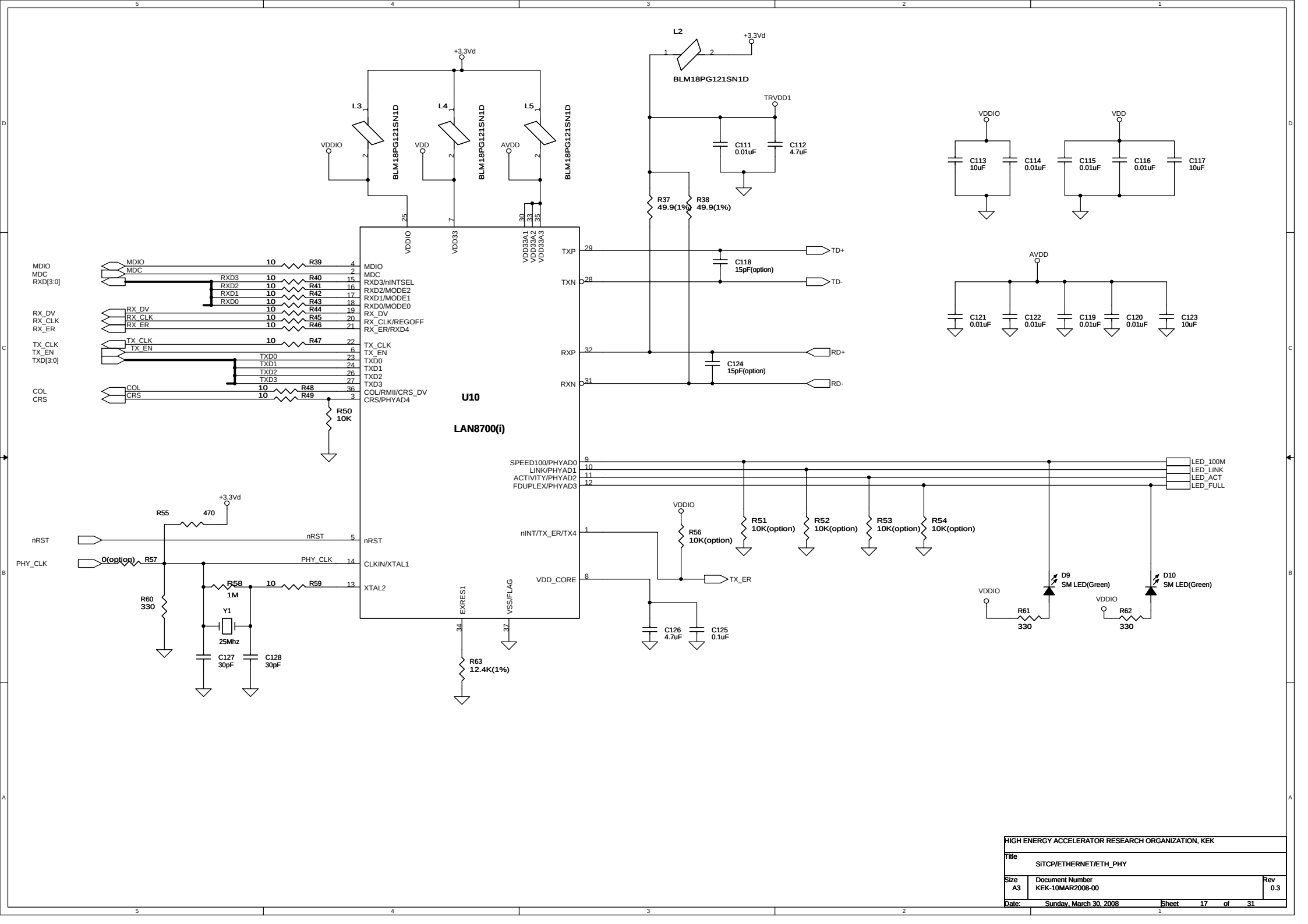




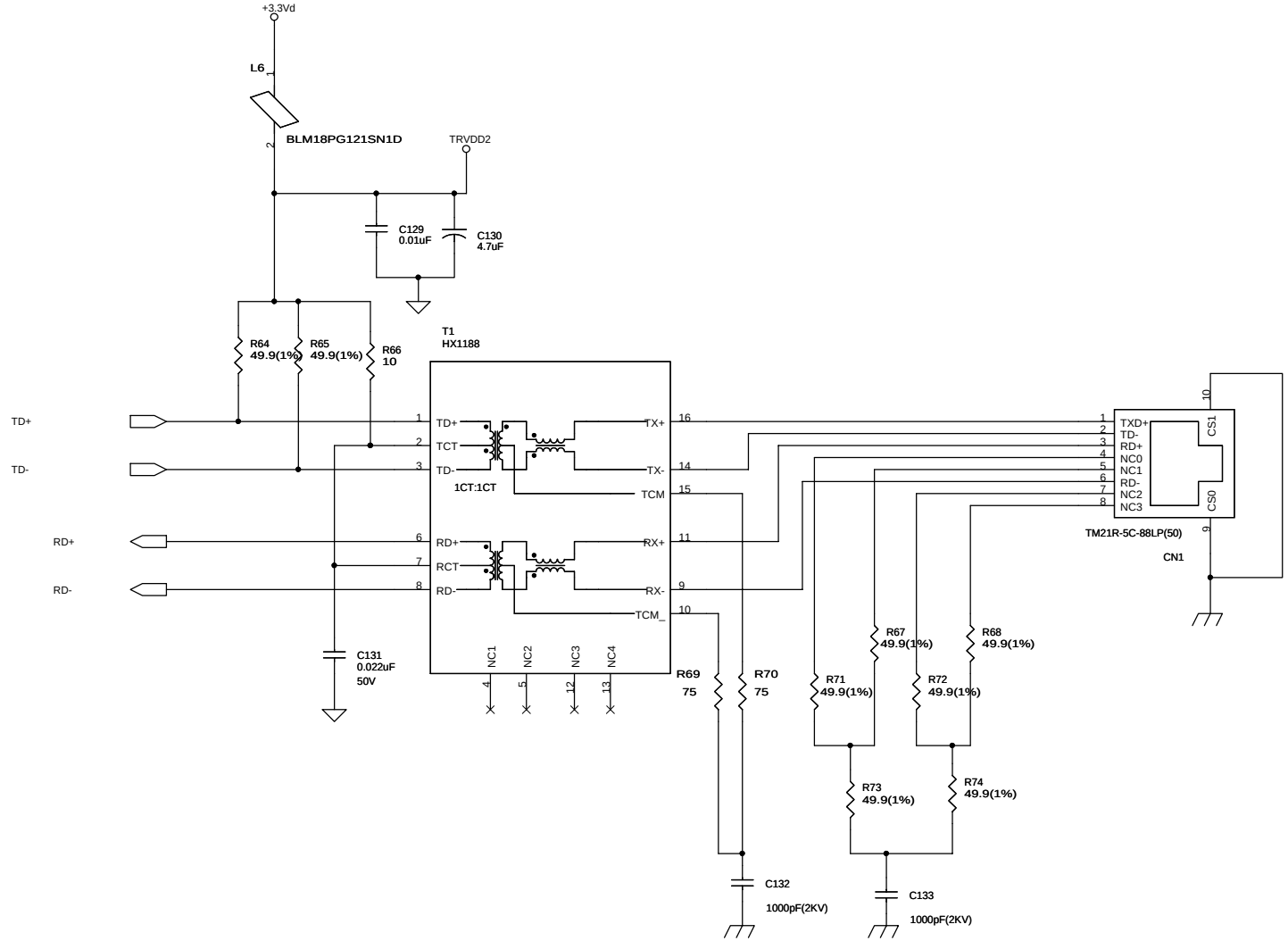




HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: MAIN/CNT_FPGA/CNT_FPGA_PWR		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 16 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION, KEK		
Title: SiTCP/ETHERNET/ETH_PHY		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Sunday, March 30, 2008	Sheet 17 of 31	



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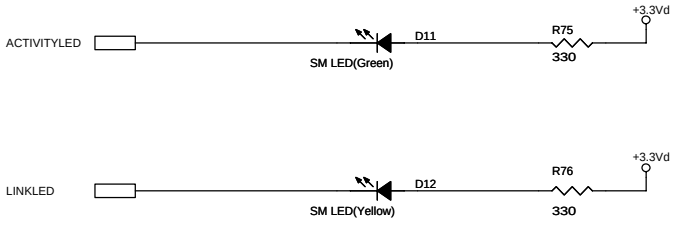
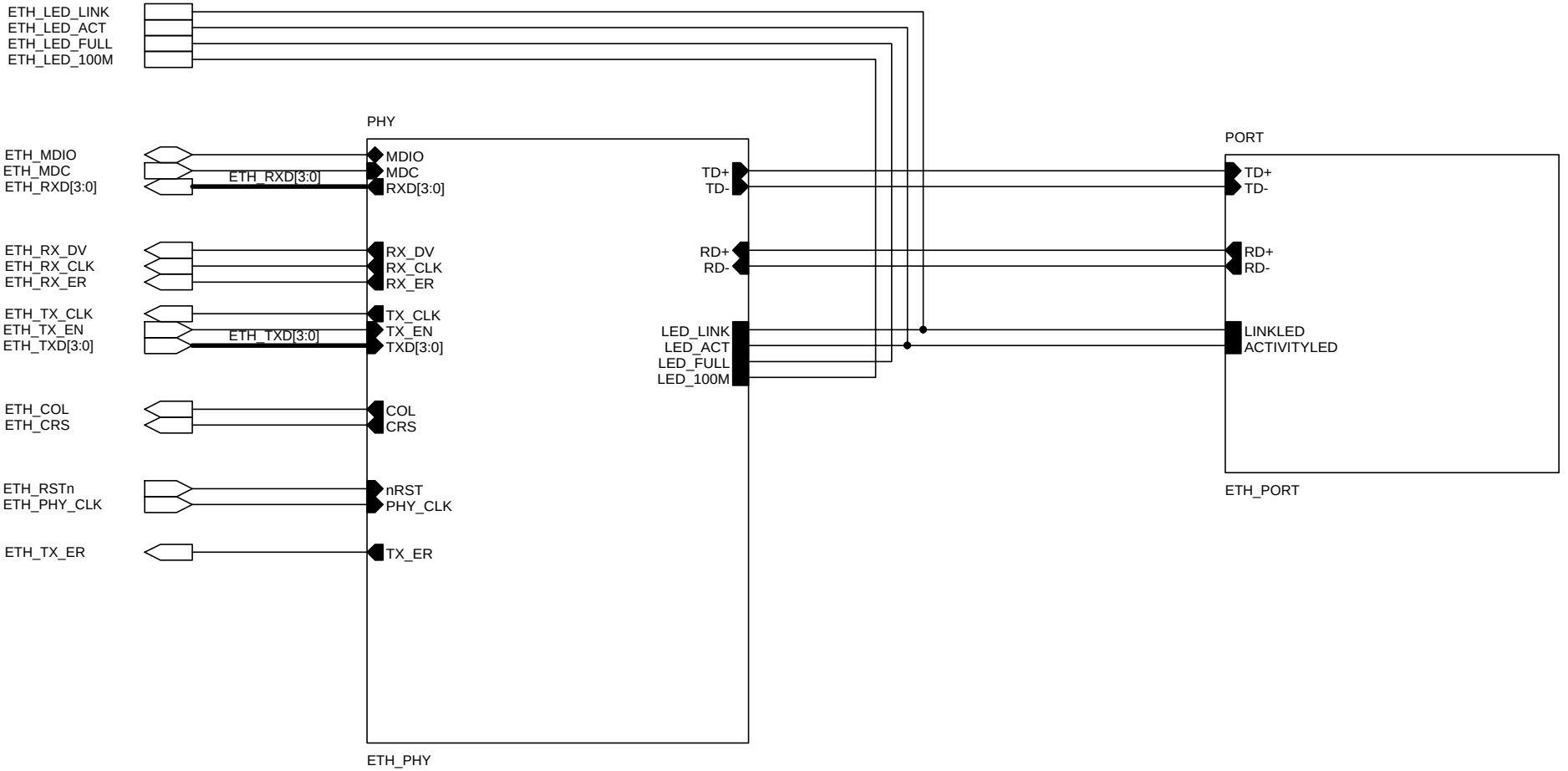
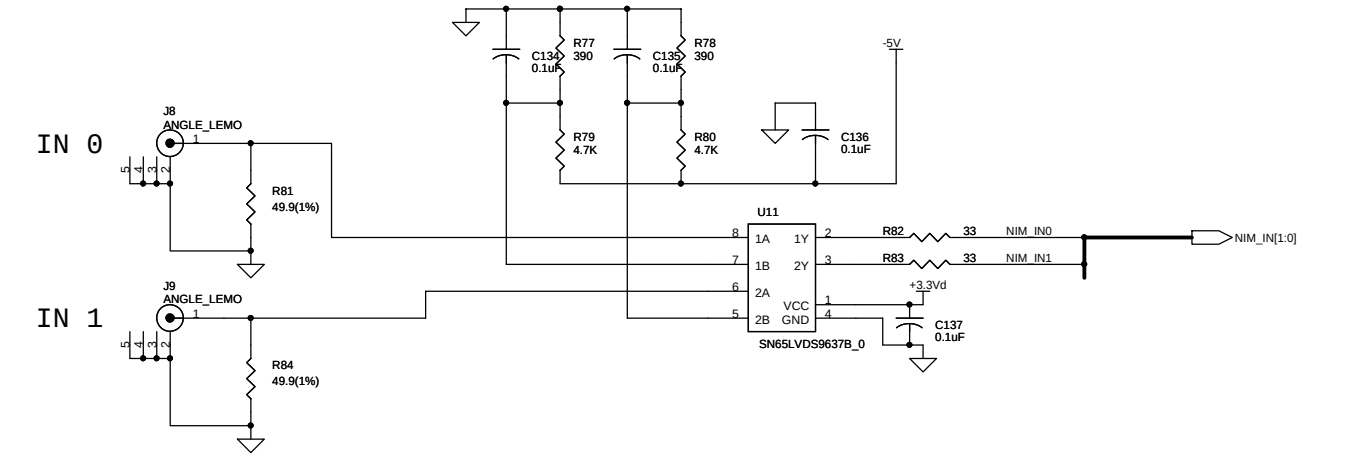
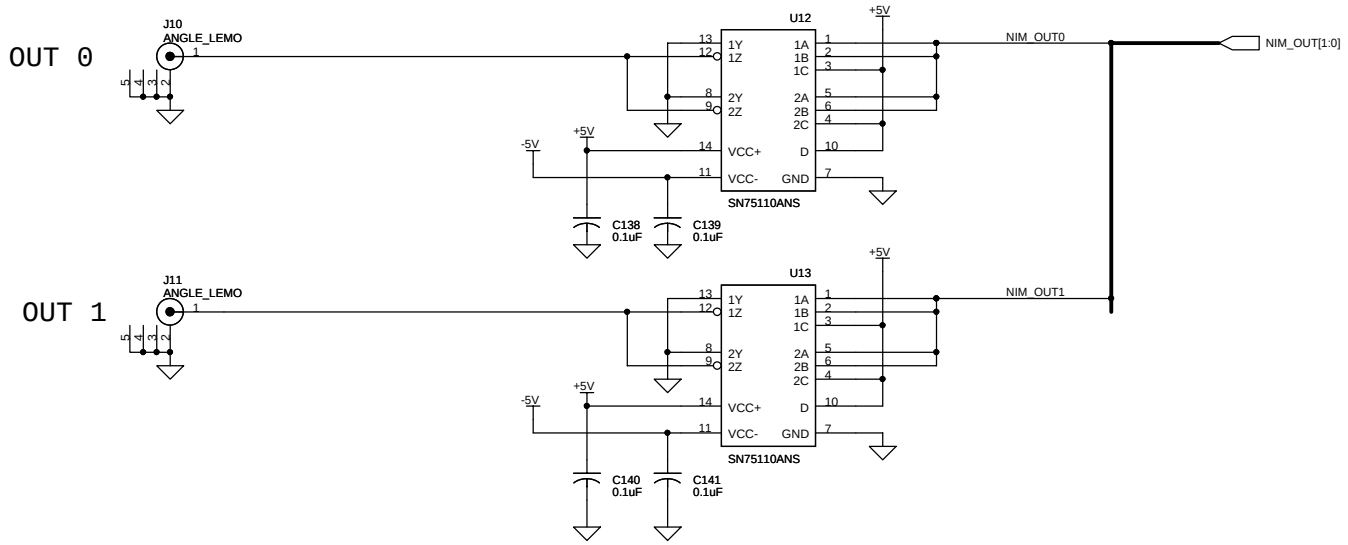


HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION, KEK		
Title: SiTCP/ETHERNET/ETH_PORT		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Sunday, March 30, 2008	Sheet 18 of 31	

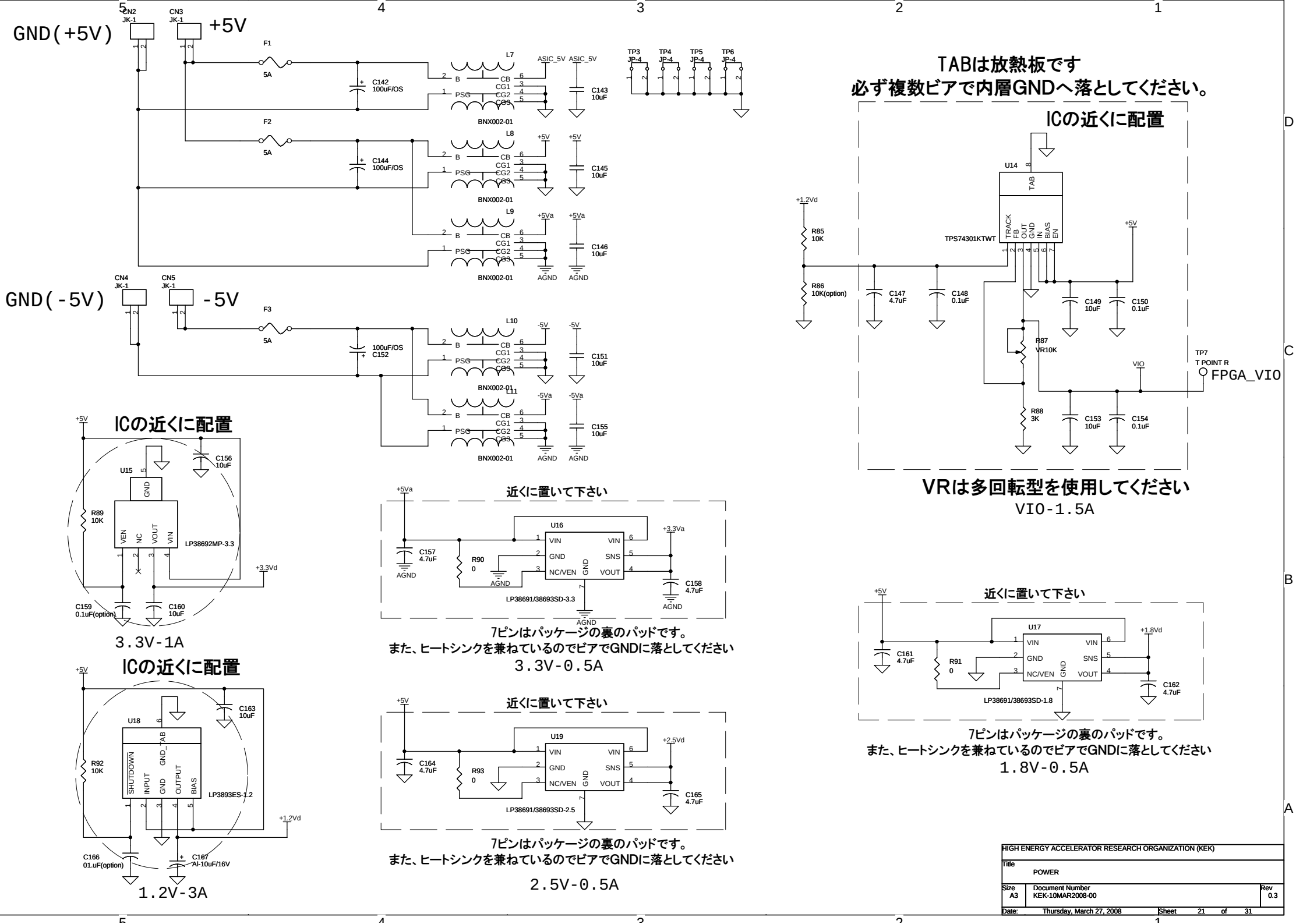


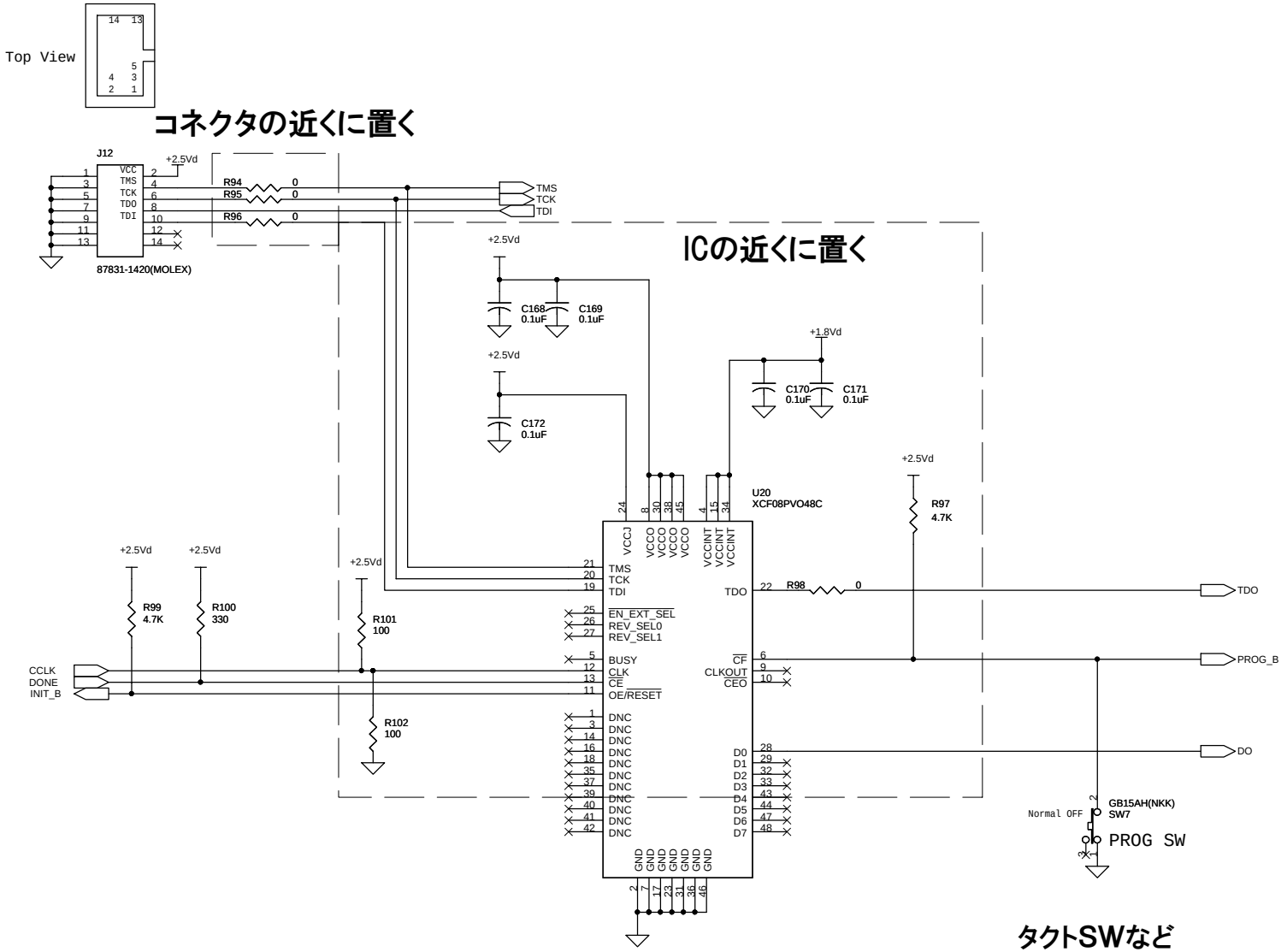
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION, KEK		
Title: SiTCP/ETHERNET		
Size: A4	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 19 of 31	



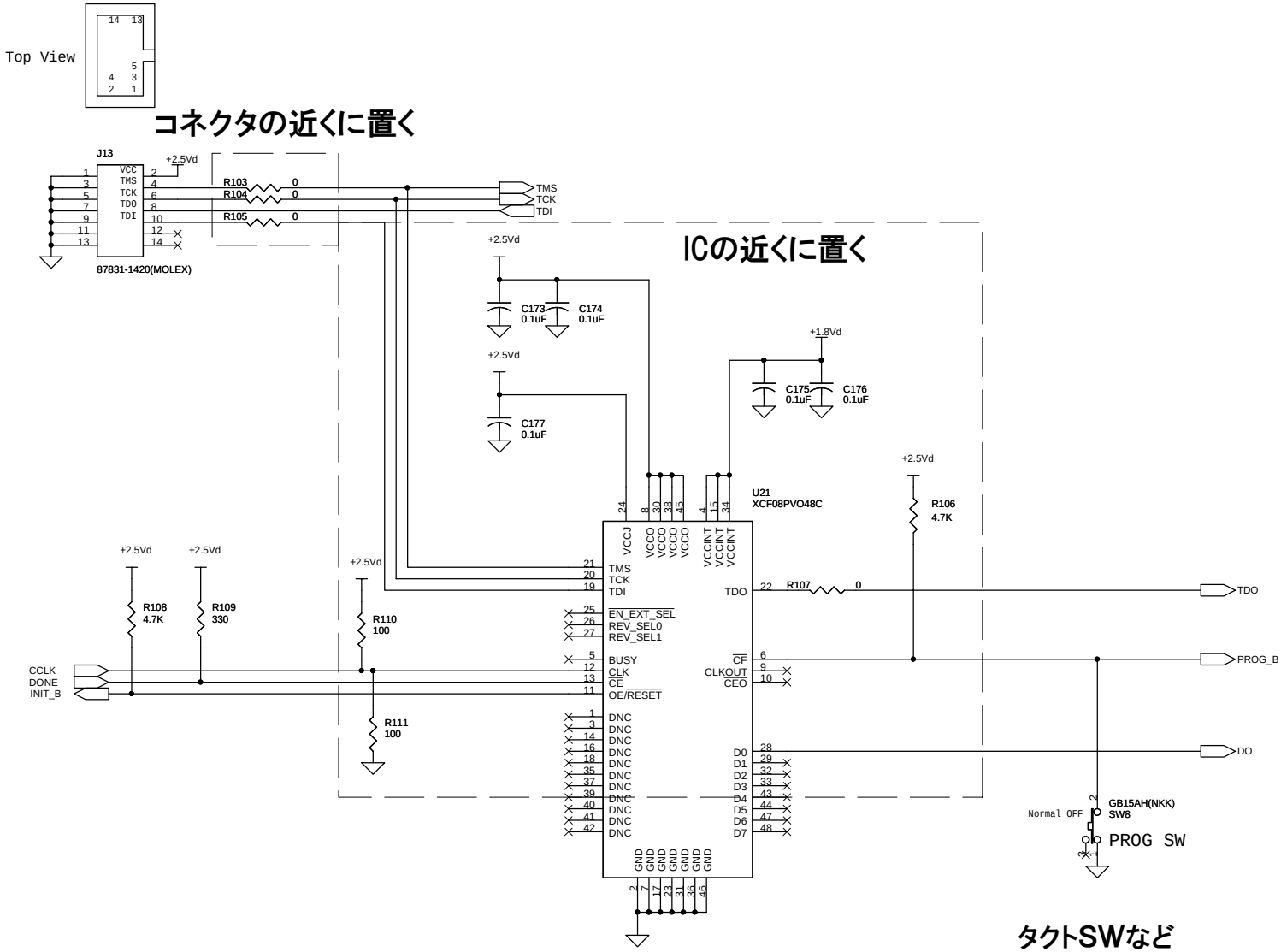


HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION, KEK		
Title: NIM_IO		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 20 of 31	

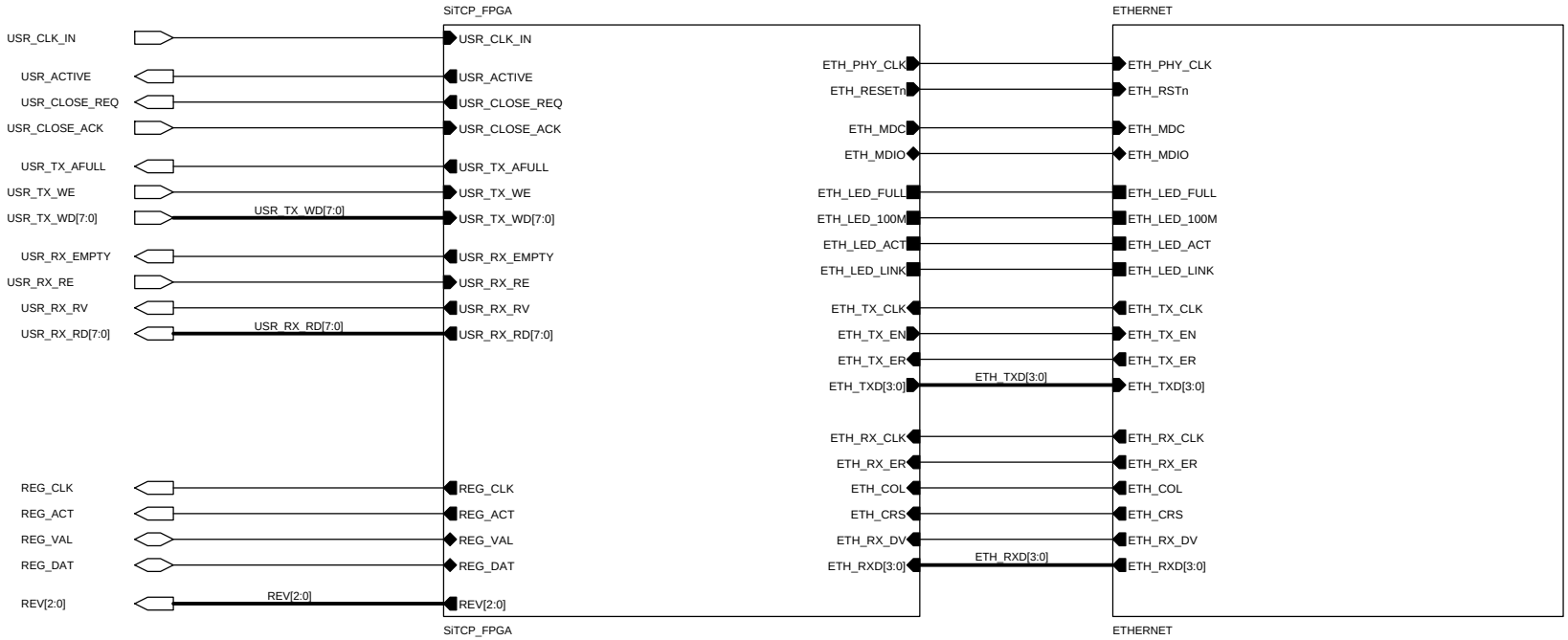

GND(+5V)
+5V
CN2 JK-1
CN3 JK-1
F1
5A
C142 100uF/OS
L7
BNX002-01
ASIC_5V
C143 10uF
F2
5A
C144 100uF/OS
L8
BNX002-01
+5V
C145 10uF
L9
BNX002-01
+5Va
AGND
C146 10uF
TP3 JP-4
TP4 JP-4
TP5 JP-4
TP6 JP-4
GND(-5V)
-5V
CN4 JK-1
CN5 JK-1
F3
5A
100uF/OS C152
L10
BNX002-01
-5V
C151 10uF
L11
BNX002-01
-5Va
C155 10uF
TABは放熱板です
必ず複数ビアで内層GNDへ落としてください。
ICの近くに配置
U14
TAB
TPS74301KTWT
TRACK
FB
OUT
GND
IN
BIAS
EN
+1.2Vd
R85 10K
R86 10K(option)
C147 4.7uF
C148 0.1uF
C149 10uF
C150 0.1uF
R87 VR10K
VIO
TP7
T POINT R
FPGA_VIO
R88 3K
C153 10uF
C154 0.1uF
VRは多回転型を使用してください
VIO-1.5A
ICの近くに配置
U15
GND
LP38692MP-3.3
VEN
NC
VOUT
VIN
R89 10K
C156 10uF
C159 0.1uF(option)
C160 10uF
+3.3Vd
3.3V-1A
近くに置いて下さい
U16
LP38691/38693SD-3.3
VIN
GND
NC/VEN
SNS
VOUT
C157 4.7uF
R90 0
C158 4.7uF
+3.3Va
7ピンはパッケージの裏のパッドです。
また、ヒートシンクを兼ねているのでビアでGNDに落としてください
3.3V-0.5A
近くに置いて下さい
U17
LP38691/38693SD-1.8
C161 4.7uF
R91 0
C162 4.7uF
+1.8Vd
7ピンはパッケージの裏のパッドです。
また、ヒートシンクを兼ねているのでビアでGNDに落としてください
1.8V-0.5A
ICの近くに配置
U18
TAB
SHUTDOWN
INPUT
GND
OUTPUT
BIAS
LP3893ES-1.2
R92 10K
C163 10uF
C166 01.uF(option)
C167 Al-10uF/16V
+1.2Vd
1.2V-3A
近くに置いて下さい
U19
LP38691/38693SD-2.5
C164 4.7uF
R93 0
C165 4.7uF
+2.5Vd
7ピンはパッケージの裏のパッドです。
また、ヒートシンクを兼ねているのでビアでGNDに落としてください
2.5V-0.5A
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)
Title
POWER
Size A3
Document Number KEK-10MAR2008-00
Rev 0.3
Date: Thursday, March 27, 2008
Sheet 21 of 31



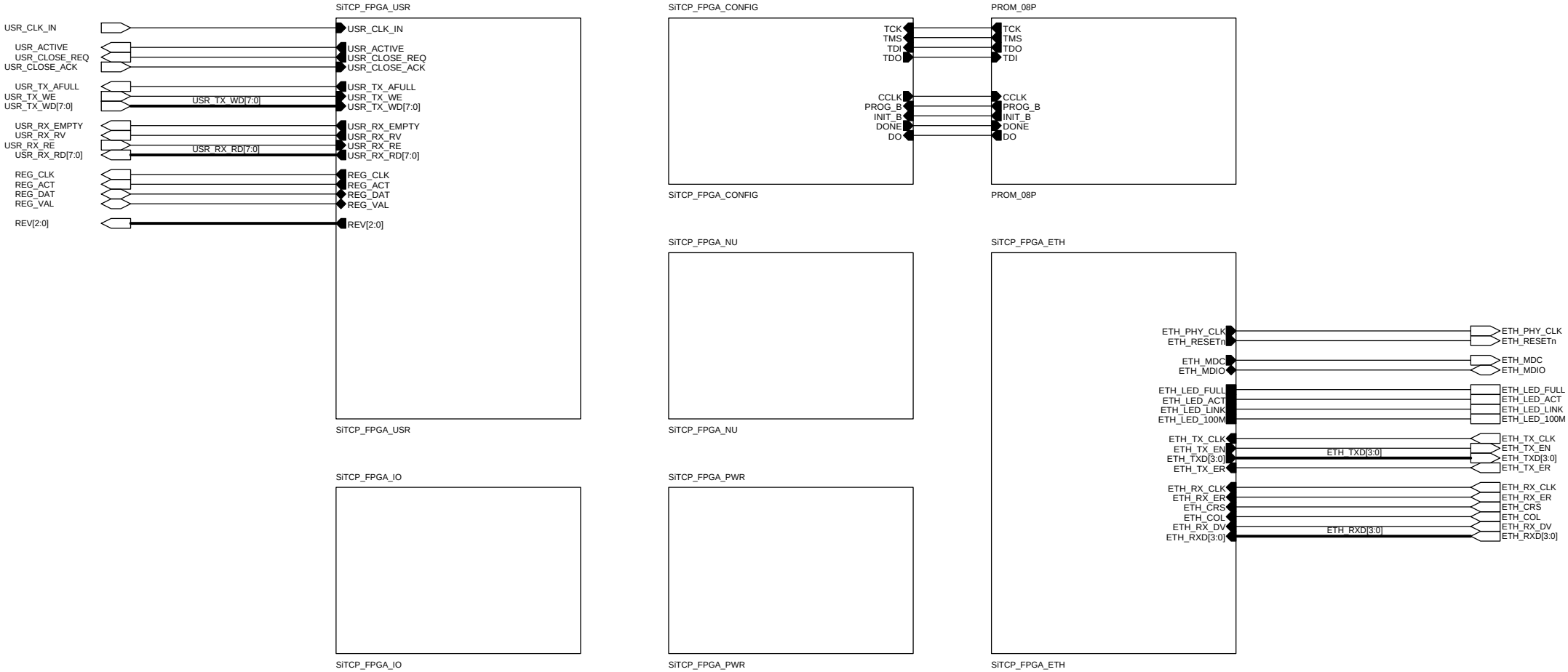
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: PROM_08P		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 24, 2008	Sheet 22 of 31	



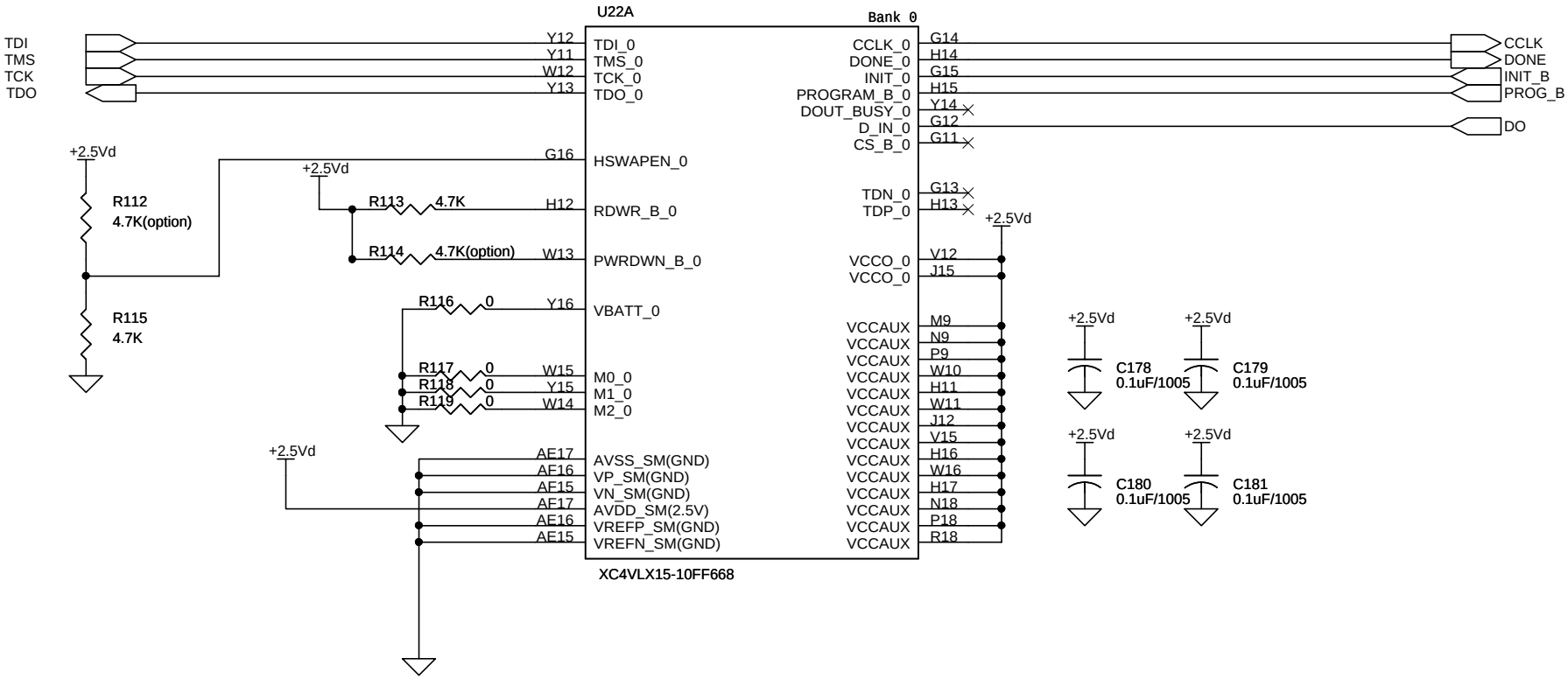
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: PROM_08P		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 24, 2008	Sheet 23 of 31	



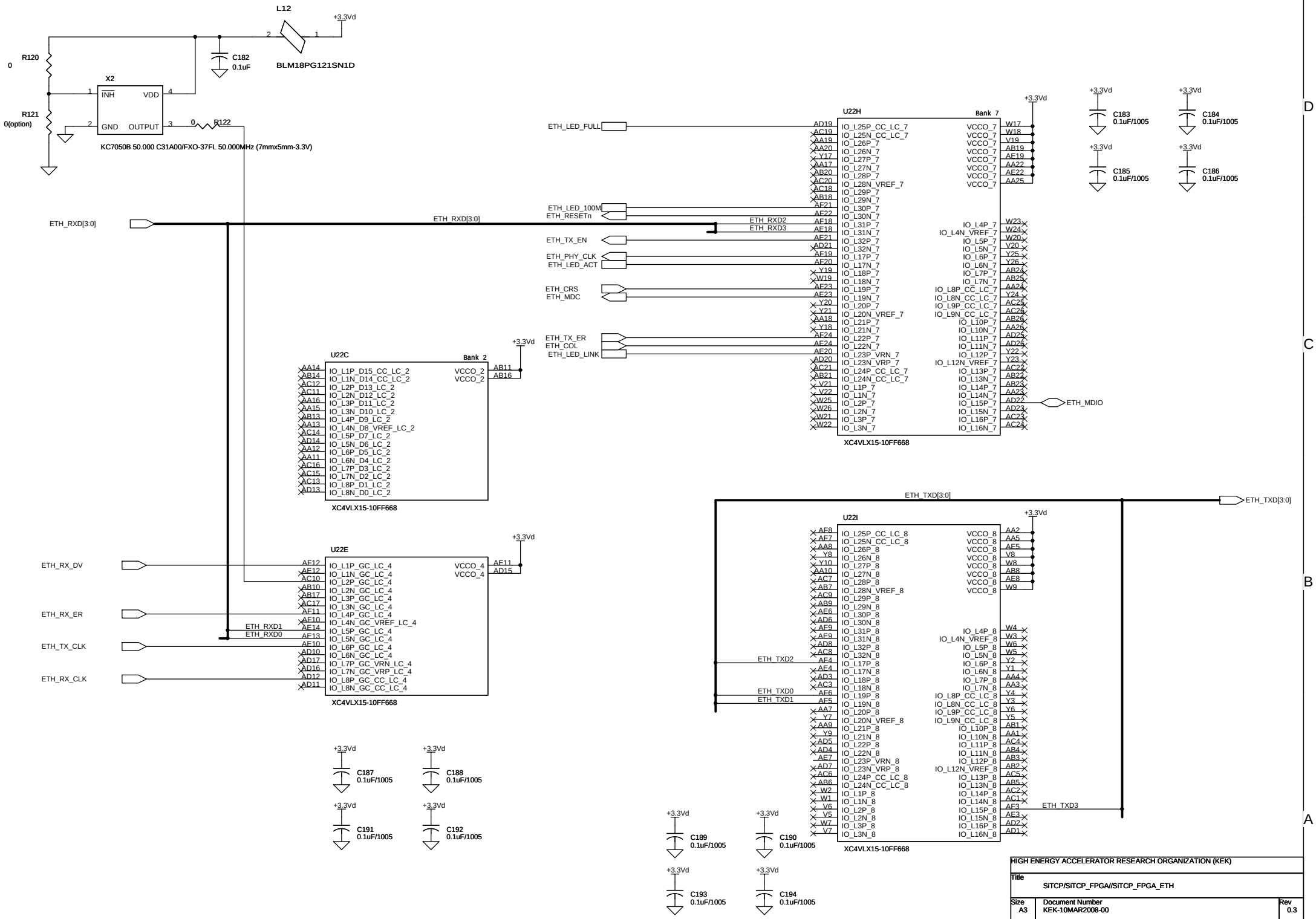
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 24 of 31	

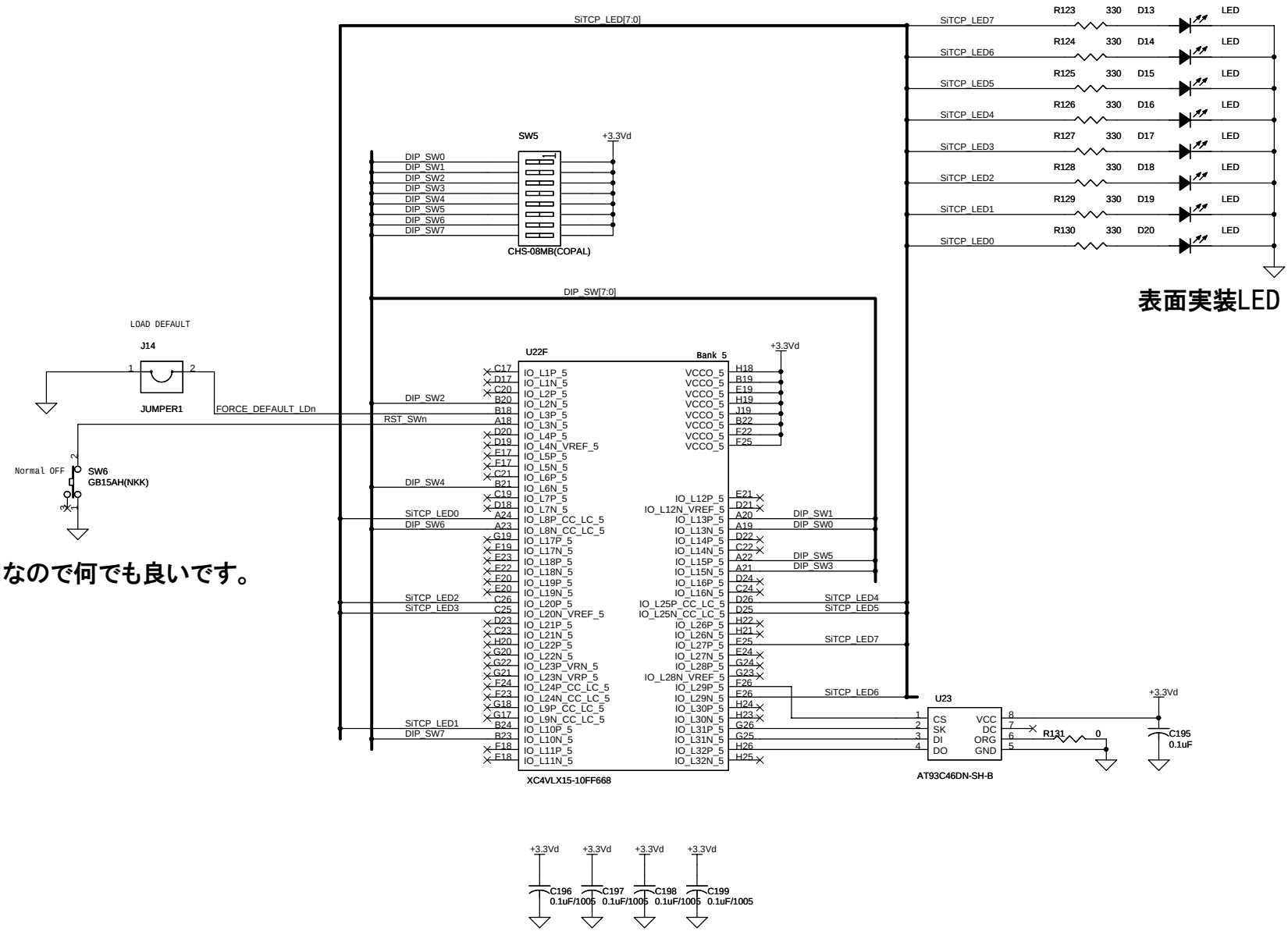


HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP/SiTCP_FPGA		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Monday, March 17, 2008	Sheet 25 of 31	

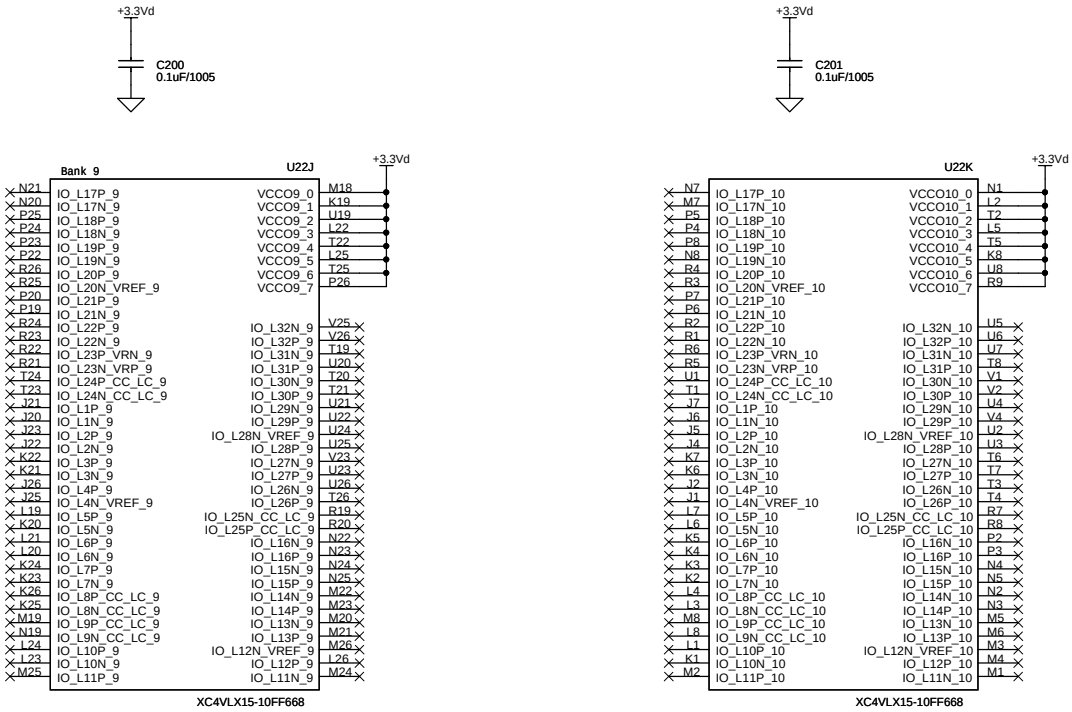


HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP/SiTCP_FPGA/SiTCP_FPGA_BANK0		
Size: A4	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 26 of 31	


L12
BLM18PG121SN1D
+3.3Vd
R120
0
C182
0.1uF
X2
INH
VDD
GND
OUTPUT
R121
0(option)
R122
KC7050B 50.000 C31A00/FXO-37FL 50.000MHz (7mmx5mm-3.3V)
ETH_RXD[3:0]
ETH_LED_FULL
ETH_LED_100M
ETH_RESETn
ETH_RXD2
ETH_RXD3
ETH_TX_EN
ETH_PHY_CLK
ETH_LED_ACT
ETH_CRS
ETH_MDC
ETH_TX_ER
ETH_COL
ETH_LED_LINK
U22H
Bank 7
XC4VLX15-10FF668
ETH_MDIO
C183
0.1uF/1005
C184
0.1uF/1005
C185
0.1uF/1005
C186
0.1uF/1005
U22C
Bank 2
XC4VLX15-10FF668
ETH_RX_DV
ETH_RX_ER
ETH_TX_CLK
ETH_RX_CLK
ETH_RXD1
ETH_RXD0
U22E
XC4VLX15-10FF668
C187
0.1uF/1005
C188
0.1uF/1005
C191
0.1uF/1005
C192
0.1uF/1005
ETH_TXD[3:0]
ETH_TXD2
ETH_TXD0
ETH_TXD1
ETH_TXD3
U22I
XC4VLX15-10FF668
C189
0.1uF/1005
C190
0.1uF/1005
C193
0.1uF/1005
C194
0.1uF/1005
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)
Title
SiTCP/SiTCP_FPGA//SiTCP_FPGA_ETH
Size
A3
Document Number
KEK-10MAR2008-00
Rev
0.3
Date:
Thursday, March 27, 2008
Sheet
27
of
31



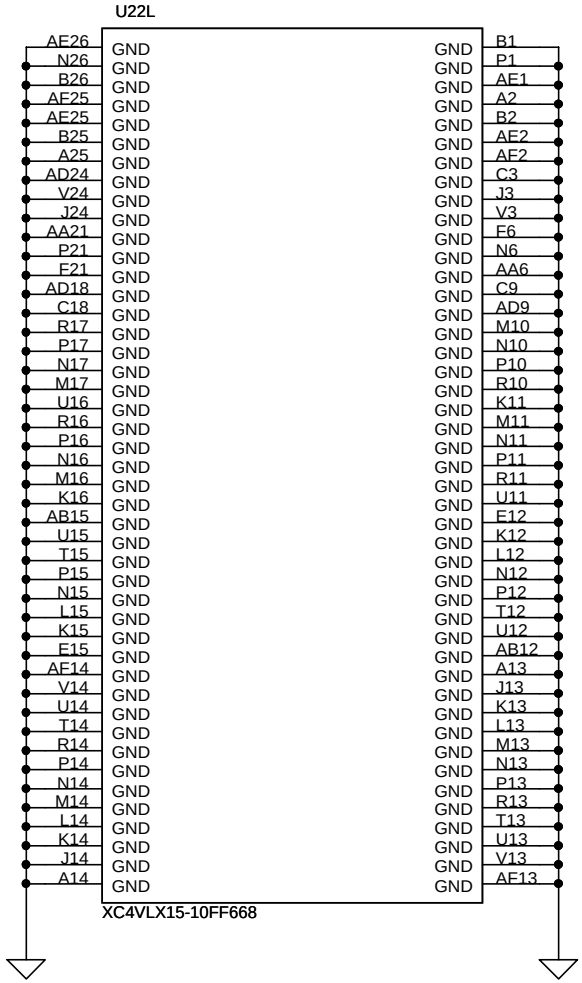
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP/SiTCP_FPGA//SiTCP_FPGA_IO		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 28 of 31	

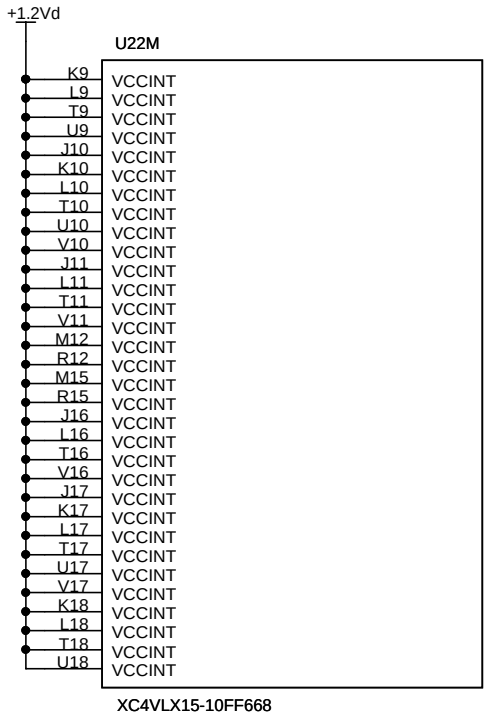


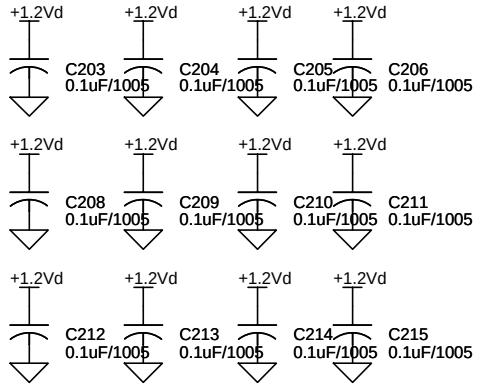
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP/SiTCP_FPGA/SiTCP_FPGA_NU		
Size: A3	Document Number: KEK-10FEB2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 29 of 31	

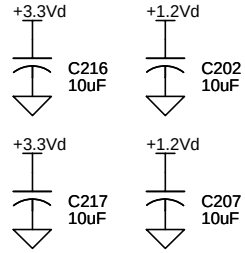
パスコンは多めに置いてあります。

無理しておく必要はありませんので、厳しい時は連絡ください

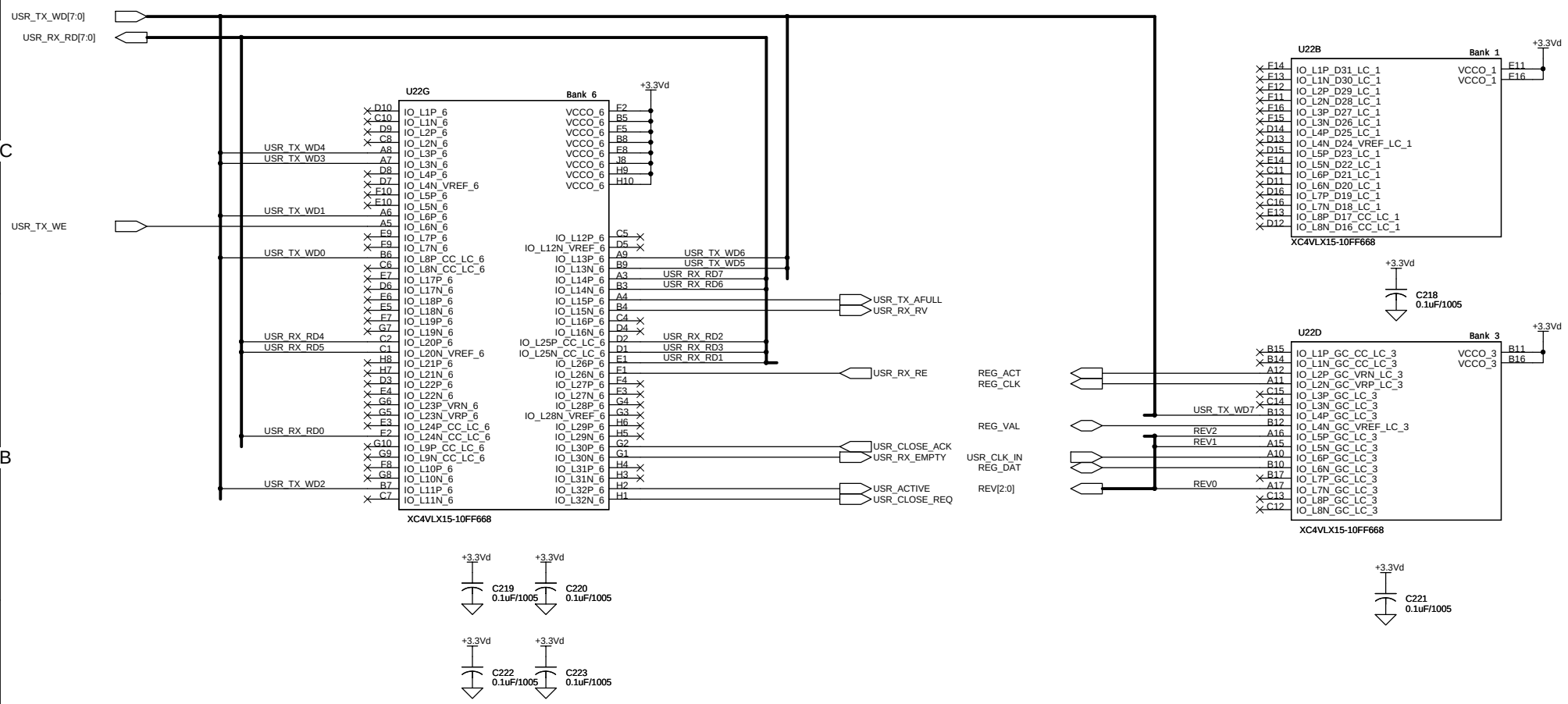








HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: ETH_FPGA_PWR		
Size: A4	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 30 of 31	



HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION (KEK)		
Title: SiTCP/SiTCP_FPGA/SiTCP_FPGA_USR		
Size: A3	Document Number: KEK-10MAR2008-00	Rev: 0.3
Date: Thursday, March 27, 2008	Sheet 31 of 31	